ChunZheng

High-end Power Semiconductor Manufacturer

KP4200A 8200V-8500V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current		I_{TAV}	4200 A	
Repetitive peak off-state voltage		V_{DRM}	8200 – 8500 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	950 µs	
V_{DRM}, V_{RRM}, V	8200	8300	8400	8500
Voltage code	82	83	84	85
T_j, °C	5 – 110			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	4200	T_c=70 °C; 180° half-sine wave	
I_{TRMS}	RMS on-state current	A	6594	T_c=70 °C; 180° half-sine wave	
I_{TSM}	Surge on-state current	kA	90	T_j=$T_{j\,max}$	t_p = 10 ms; sine half wave; V_D = V_R= 0 V; after surge
I^2t	Safety factor	$A^2s{\cdot}10^6$	40.5	T_j=$T_{j\,max}$	t_p = 10 ms; sine half wave; V_D = V_R= 0 V; after surge
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	8200-8500	f = 50 Hz, t_p = 10 ms, t_{p1} = 250µs, $T_{j\,min}$< T_j <$T_{j\,max}$;	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	8200-8500	t_p = 10 ms, f = 5 Hz $T_{j\,min}$< T_j <$T_{j\,max}$;	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6{\cdot}V_{DRM}$ $0.6{\cdot}V_{RRM}$	T_j=$T_{j\,max}$; Gate open	

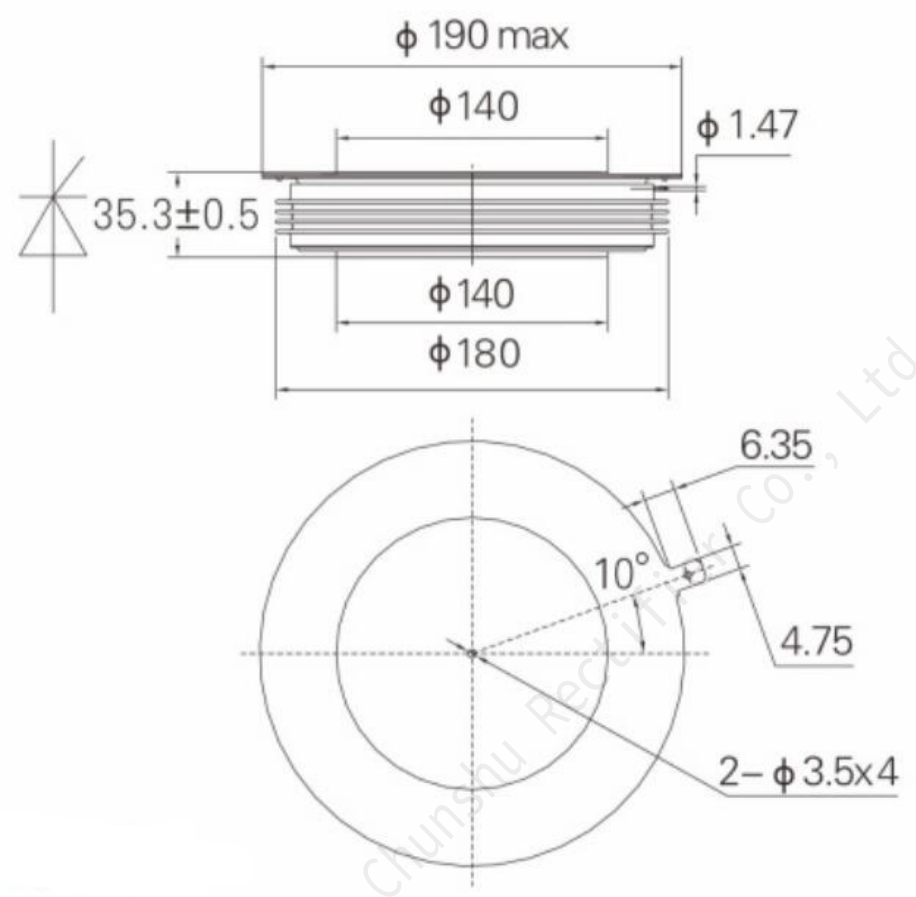
TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	10	
P_G	Gate power dissipation	W	3	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	1000	$T_j=T_{j\,max}$; $V_D \le 0.67.V_{DRM}$; I_{FG} = 5 A; t_r = 0.5 μs
THERMAL				
T_{stg}	Storage temperature	°C	-40–140	
T_j	Operating junction temperature	°C	5 –110	
MECHANICAL				
F	Mounting force	kN	170-210	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	1.90	T_j=110 °C; I_T=5000A
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	I_T = 2000 A - 6000 A
r_T	On-state slope resistance, max	mΩ	0.160	$T_j=T_{j\,max}$;
I_L	Latching current, max	mA	150	T_j=25 °C
I_H	Holding current, max	mA	1500	T_j=25 °C;
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	2000	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)]	V/μs	2000	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	2.60	T_j=25 °C
I_{GT}	Gate trigger direct current, max	mA	400	T_j= 25 °C
V_{GD}	Gate non-trigger direct voltage, min	V	0.30	$T_j=T_{j\,max}$; $V_D=0.4 \cdot V_{DRM}$; dv/dt = 2000 V/μs
I_{GD}	Gate non-trigger direct current, min	mA	10.00	
SWITCHING				
t_q	Turn-off time[2)]	μs	950	T_{vj} = 110 °C, I_{TRM} = 3000 A, V_R = 200 V, di_T/dt = -1.5 A/μs, $V_D \le 0.67.V_{DRM}$, dv_D/dt = 20 V/μs
Q_{rr}	Total recovered charge, max	μAs	9900	T_{vj} = 110 °C, I_{TRM} = 3000 A, V_R = 200 V, di_T/dt = -1.5 A/μs
I_{rrM}	Peak reverse recovery current, max	A	140	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.003	Direct current	Double side cooled
R_{thjc-A}			0.006		Anode side cooled
R_{thjc-K}			0.006		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0006	Direct current, Double side cooled	
MECHANICAL					
w	Weight, typ	g	5140		
D_s	Surface creepage distance	mm	56		
D_a	Air strike distance	mm	22		

OVERALL DIMENSIONS



KT150DT

All dimensions in millimeters

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	2.005	0.602	0.251	0.141
τ_i(s)	0.939	0.146	0.024	0.006

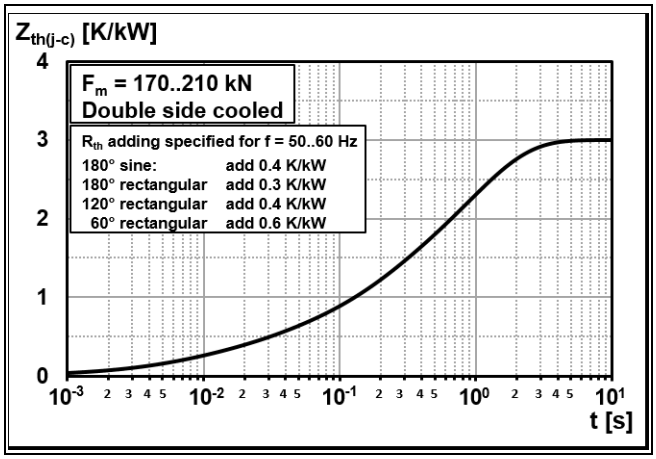


Fig. 1 Transient thermal impedance (junction-to-case) vs. time

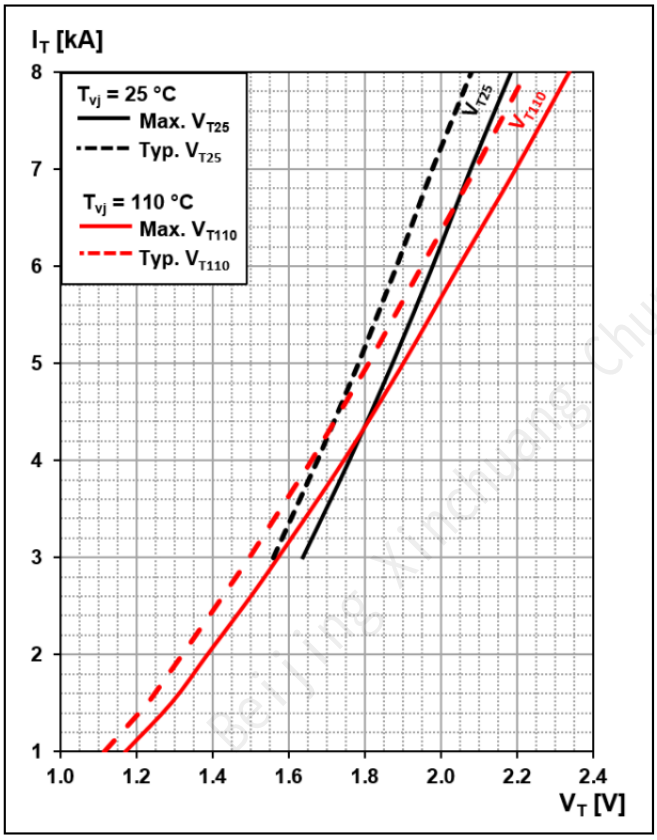


Fig. 2 On-state voltage characteristics

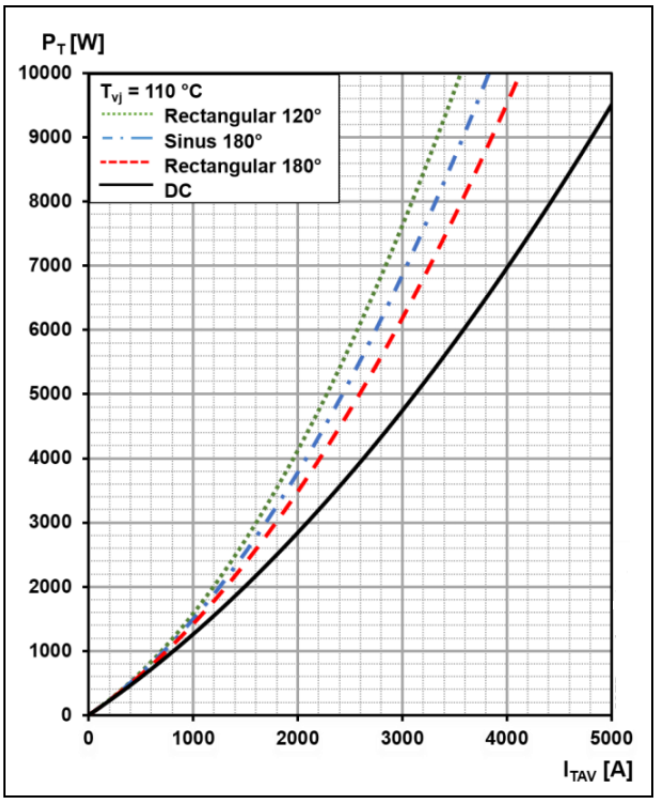


Fig. 3 On-state power dissipation vs. mean on-state current, turn-on losses excluded

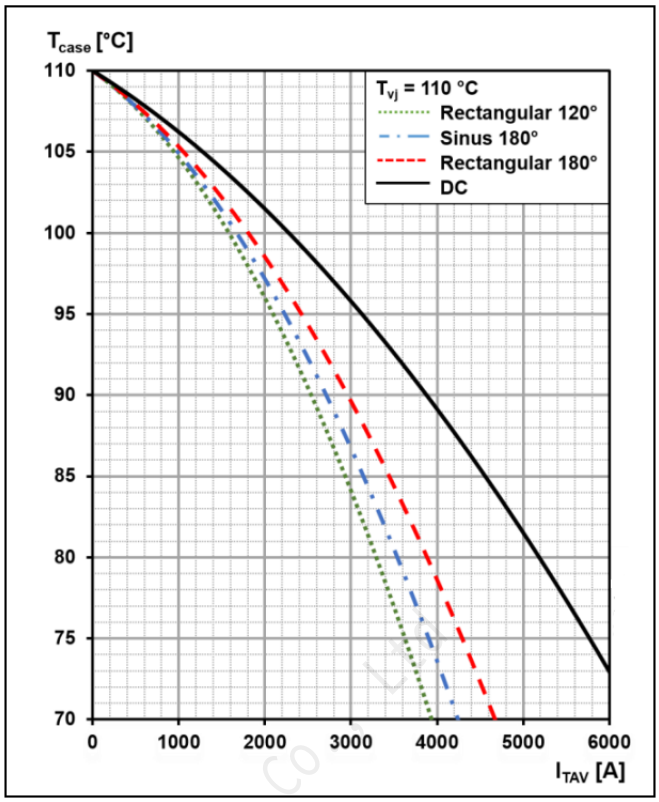


Fig. 4 Max. permissible case temperature vs. mean on-state current, switching losses ignored

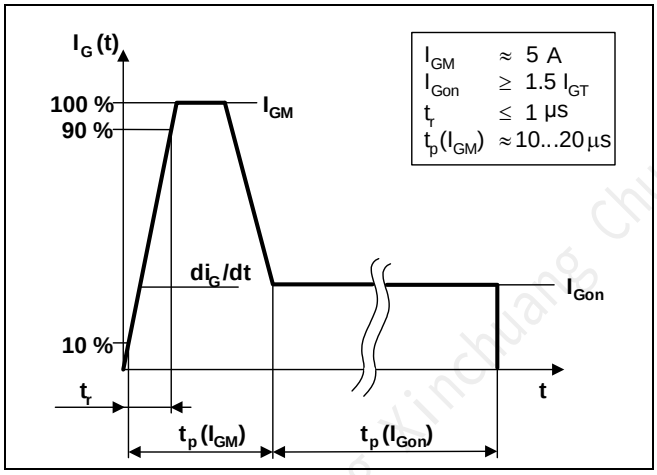


Fig. 5 Recommended gate current waveform

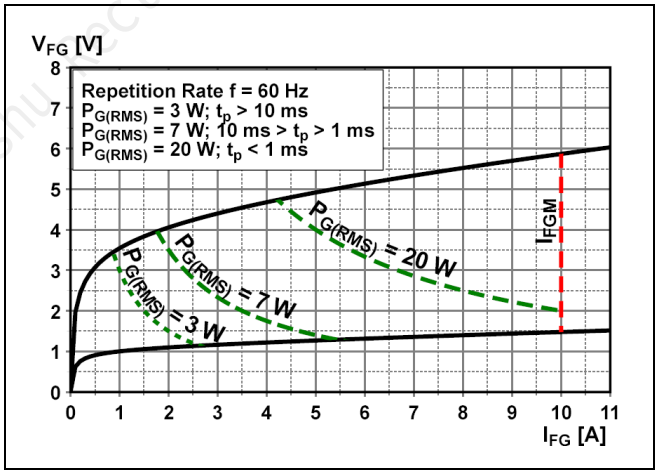


Fig. 6 Max. peak gate power loss

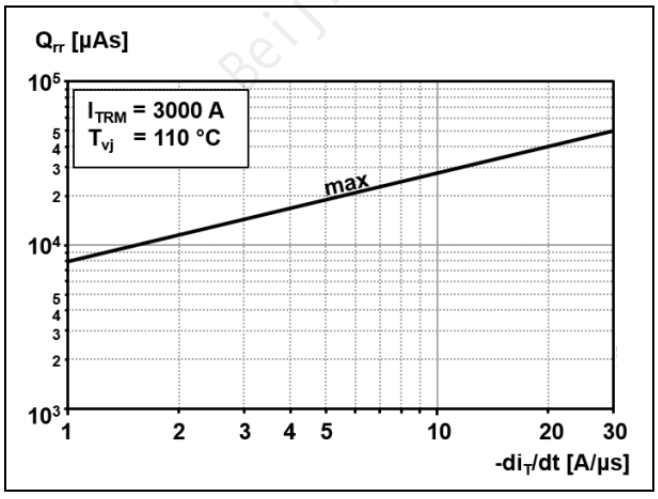


Fig. 7 Reverse recovery charge vs. decay rate of on-state current

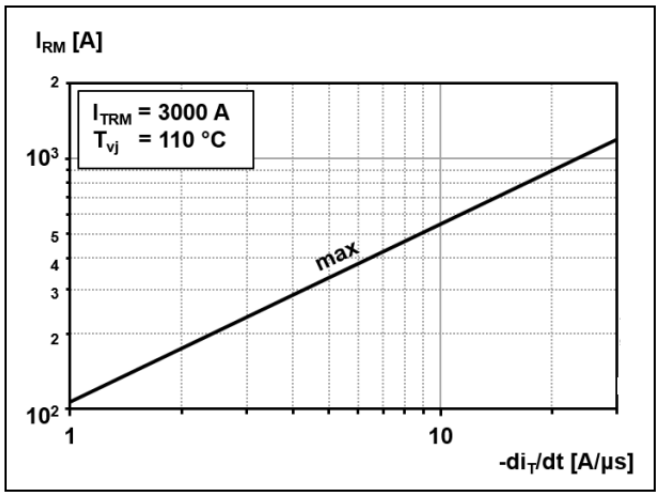


Fig. 8 Peak reverse recovery current vs. decay rate of on-state current

Power losses

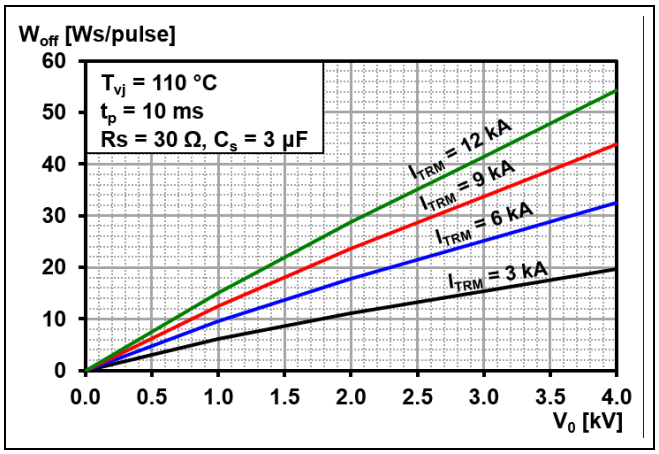


Fig. 9 Turn-off energy, half sinusoidal waves

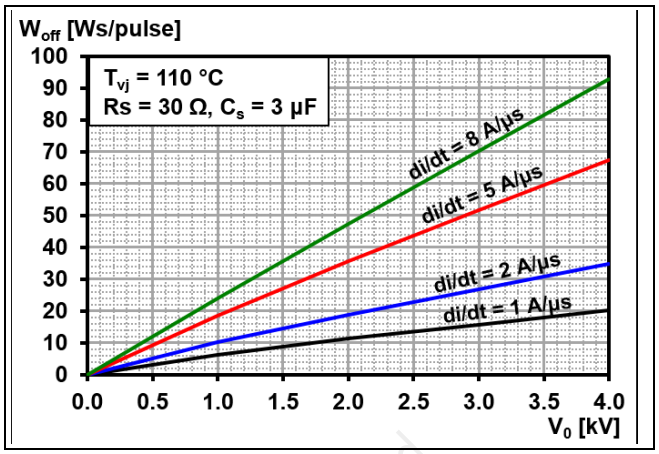


Fig. 10 Turn-off energy, rectangular waves

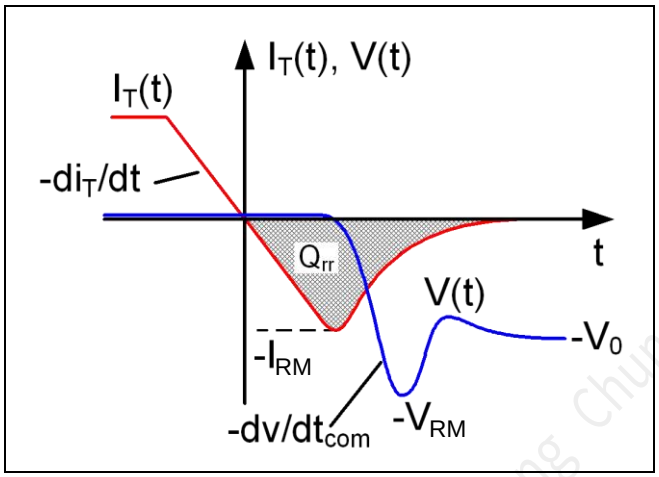


Fig. 11 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T}\int_0^T I_T \cdot V_T(I_T)\ dt$$

Fig. 12 Relationships for power loss

