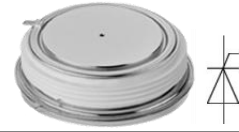




High-end Power Semiconductor Manufacturer

KP500A 4600V-6500V Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications



Mean on-state current	I_{TAV}		500 A									
Repetitive peak off-state voltage	V_{DRM}		4600 – 6500 V									
Repetitive peak reverse voltage	V_{RRM}											
Turn-off time	t_q		630 μ s									
V_{DRM}, V_{RRM}, V	4600	4800	5000	5200	5400	5600	5800	6000	6200	6400	6500	
Voltage code	46	48	50	52	54	56	58	60	62	64	65	
$T_j, ^\circ\text{C}$	-60 – 125											

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	500	$T_c=85^\circ\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	785	$T_c=85^\circ\text{C}$, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	10.5 12.1	$T_j=T_{j\max}$ $T_j=25^\circ\text{C}$	180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			11.0 12.7	$T_j=T_{j\max}$ $T_j=25^\circ\text{C}$	180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
I^2t	Safety factor	$\text{A}^2\text{s}\cdot 10^3$	551 729	$T_j=T_{j\max}$ $T_j=25^\circ\text{C}$	180° half-sine wave; 50 Hz ($t_p=10$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
			504 667	$T_j=T_{j\max}$ $T_j=25^\circ\text{C}$	180° half-sine wave; 60 Hz ($t_p=8.3$ ms); single pulse; $V_D=V_R=0$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μ s; $di_G/dt \geq 1$ A/ μ s
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600–6500	$T_{j\min} < T_j < T_{j\max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700–6600	$T_{j\min} < T_j < T_{j\max}$; 180° half-sine wave; 50 Hz; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.75V_{DRM}$ $0.75V_{RRM}$	$T_j=T_{j\max}$; Gate open	

TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j = T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j = T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/ μ s	630	$T_j = T_{j\ max}; V_D = 0.67 \cdot V_{DRM}; I_{TM} = 2 I_{TAV};$ Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s
THERMAL				
T_{stg}	Storage temperature	$^{\circ}$ C	-60 –125	
T_j	Operating junction temperature	$^{\circ}$ C	-60 –125	
MECHANICAL				
F	Mounting force	kN	24.0 –28.0	
a	Acceleration	m/s ²	50 100	Device unclamped Device clamped

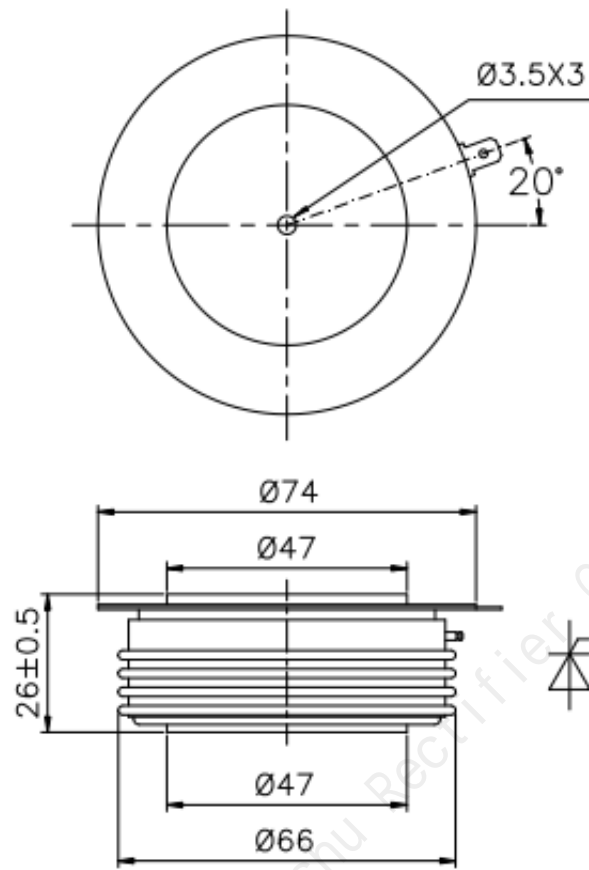
CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.70	$T_j = 25 \text{ }^{\circ}\text{C}; I_{TM} = 1570$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	$T_j = T_{j\ max};$	
r_T	On-state slope resistance, max	m Ω	1.070	$0.5 \pi I_{TAV} < I_T < 1.5 \pi I_{TAV}$	
I_L	Latching current, max	mA	1500	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 12$ V; Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
I_H	Holding current, max	mA	300	$T_j = 25 \text{ }^{\circ}\text{C};$ $V_D = 12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j = T_{j\ max};$ $V_D = V_{DRM}; V_R = V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage ¹⁾ , min	V/ μ s	1000	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$ Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.00	$T_j = 25 \text{ }^{\circ}\text{C}$ $T_j = T_{j\ max}$	$V_D = 12$ V; $I_D = 3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	300 200	$T_j = 25 \text{ }^{\circ}\text{C}$ $T_j = T_{j\ max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j = T_{j\ max};$ $V_D = 0.67 \cdot V_{DRM};$	
I_{GD}	Gate non-trigger direct current, min	mA	15.00	Direct gate current	
SWITCHING					
t_{gd}	Delay time	μ s	4.00	$T_j = 25 \text{ }^{\circ}\text{C}; V_D = 0.4 \cdot V_{DRM}; I_{TM} = I_{TAV};$ Gate pulse: $I_G = 2$ A; $t_{GP} = 50 \mu$ s; $di_G/dt \geq 1$ A/ μ s	
t_q	Turn-off time ²⁾ , max	μ s	630	$dv_D/dt = 50$ V/ μ s; $T_j = T_{j\ max}; I_{TM} = I_{TAV};$ $di_R/dt = -10$ A/ μ s; $V_R = 100$ V; $V_D = 0.67 \cdot V_{DRM}$	
Q_{rr}	Total recovered charge, max	μ C	4500	$T_j = T_{j\ max}; I_{TM} = 2000$ A;	
t_{rr}	Reverse recovery time, typ	μ s	60.0	$di_R/dt = -5$ A/ μ s;	
I_{rrM}	Peak reverse recovery current, max	A	150	$V_R = 100$ V	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0180	Direct current	Double side cooled
R_{thjc-A}			0.0396		Anode side cooled
R_{thjc-K}			0.0324		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0040	Direct current	
MECHANICAL					
w	Weight, typ	g	510		
D_s	Surface creepage distance	mm (inch)	31.60 (1.244)		
D_a	Air strike distance	mm (inch)	16.50 (0.649)		

Beijing Xinchuang Chunshu Rectifier Co., Ltd

OVERALL DIMENSIONS



KT55

All dimensions in millimeters

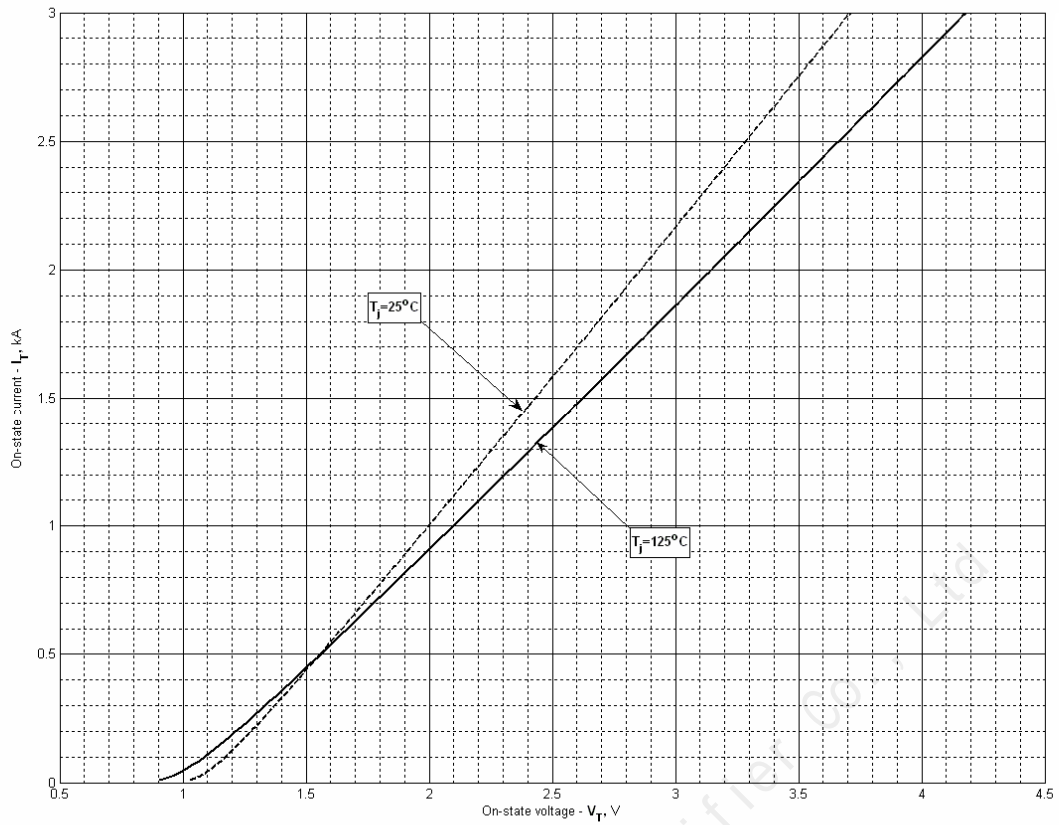


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	$T_j = 25^\circ\text{C}$	$T_j = T_{j\text{max}}$
A	1.000464	0.867399
B	0.809489	0.979250
C	-0.230666	-0.308071
D	0.347401	0.463978

On-state characteristic model (see Fig. 1)

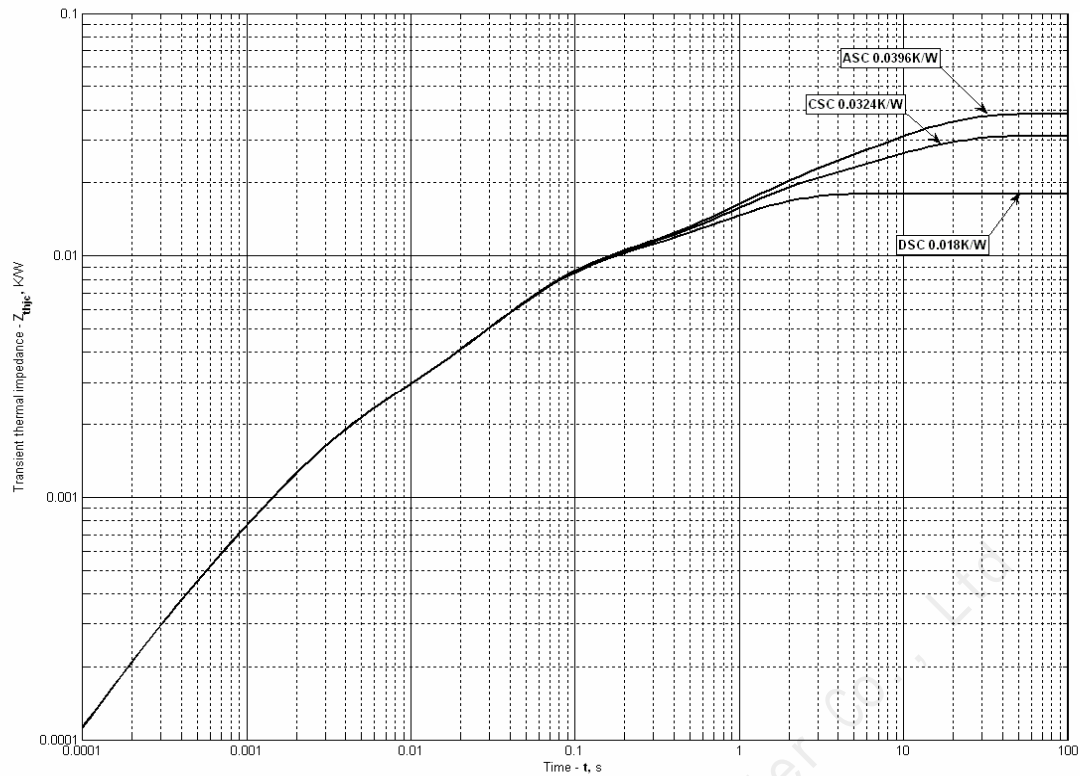


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^n R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where $i = 1$ to n , n is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t .

R_i = Amplitude of p_{th} term.

τ_i = Time constant of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i K/W	0.009241	0.006037	0.001231	0.001054	0.0003396	0.00009575
τ_i s	0.9673	0.04967	0.002733	0.07734	0.001638	0.0002248

DC Cathode side cooled

i	1	2	3	4	5	6
R_i K/W	0.01318	0.009281	0.006055	0.001018	0.001535	0.0001182
τ_i s	9.745	1.028	0.05591	0.03732	0.002468	0.0002687

DC Anode side cooled

i	1	2	3	4	5	6
R_i K/W	0.02041	0.009325	0.006949	0.0001252	0.001516	0.0001119
τ_i s	9.752	1.065	0.05344	0.01407	0.002421	0.0002554

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

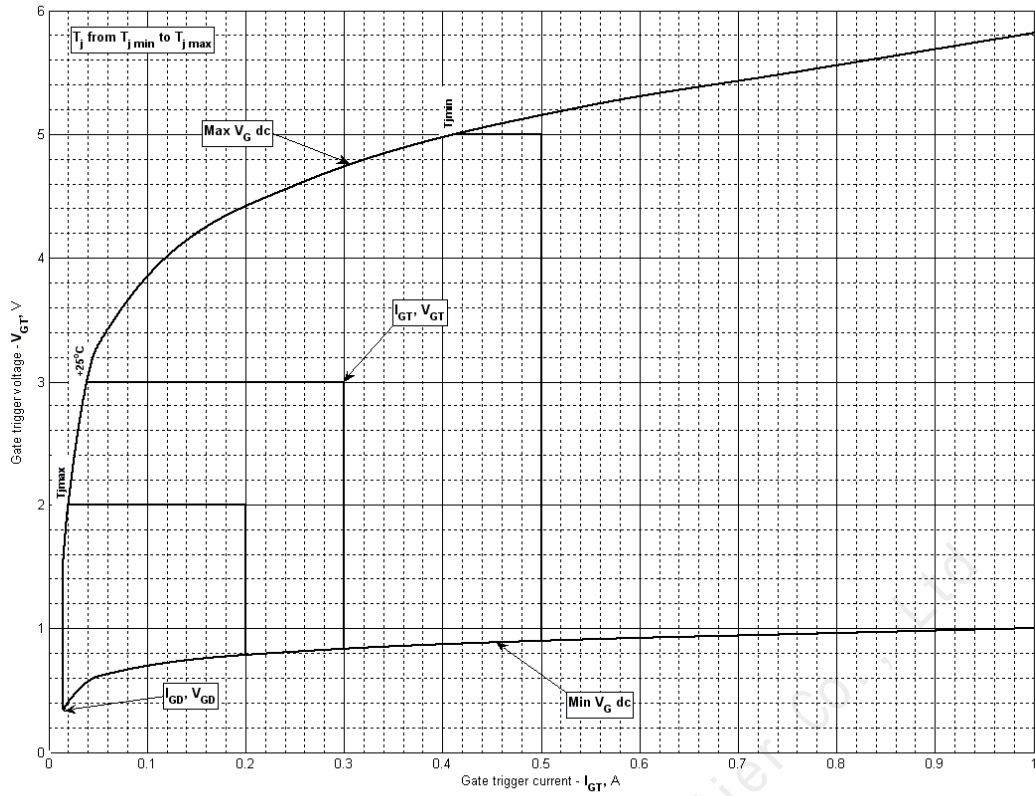


Fig 3 – Gate characteristics – Trigger limits

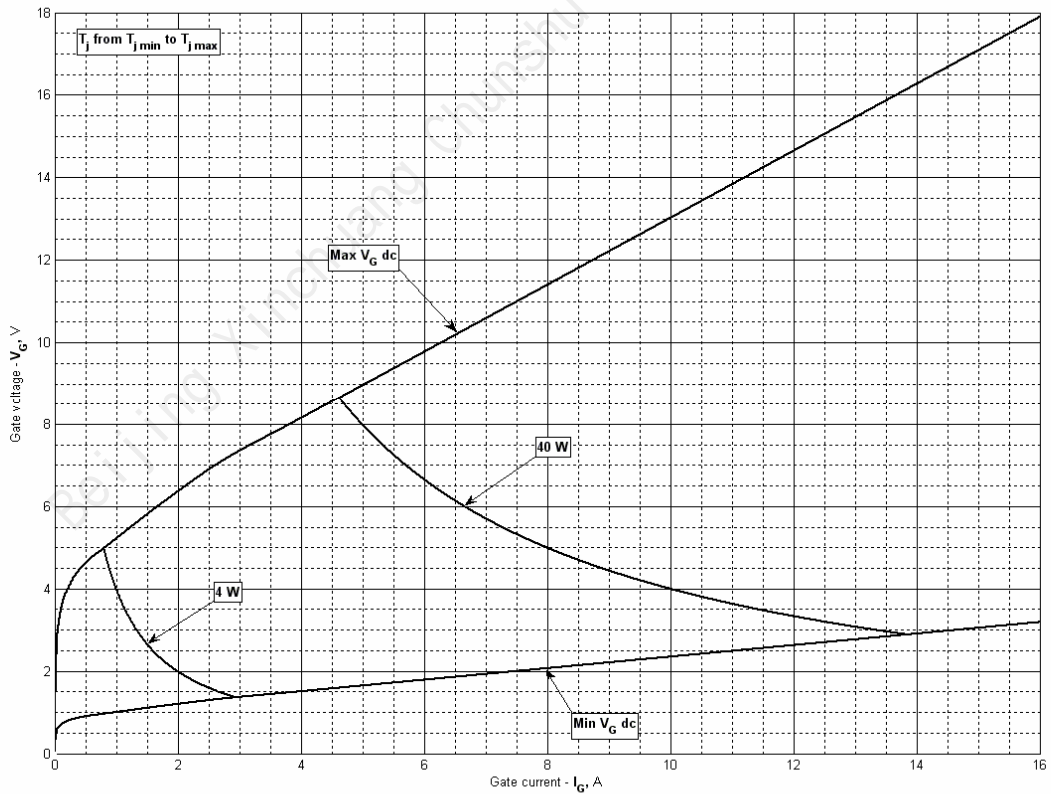


Fig 4 - Gate characteristics –Power curves

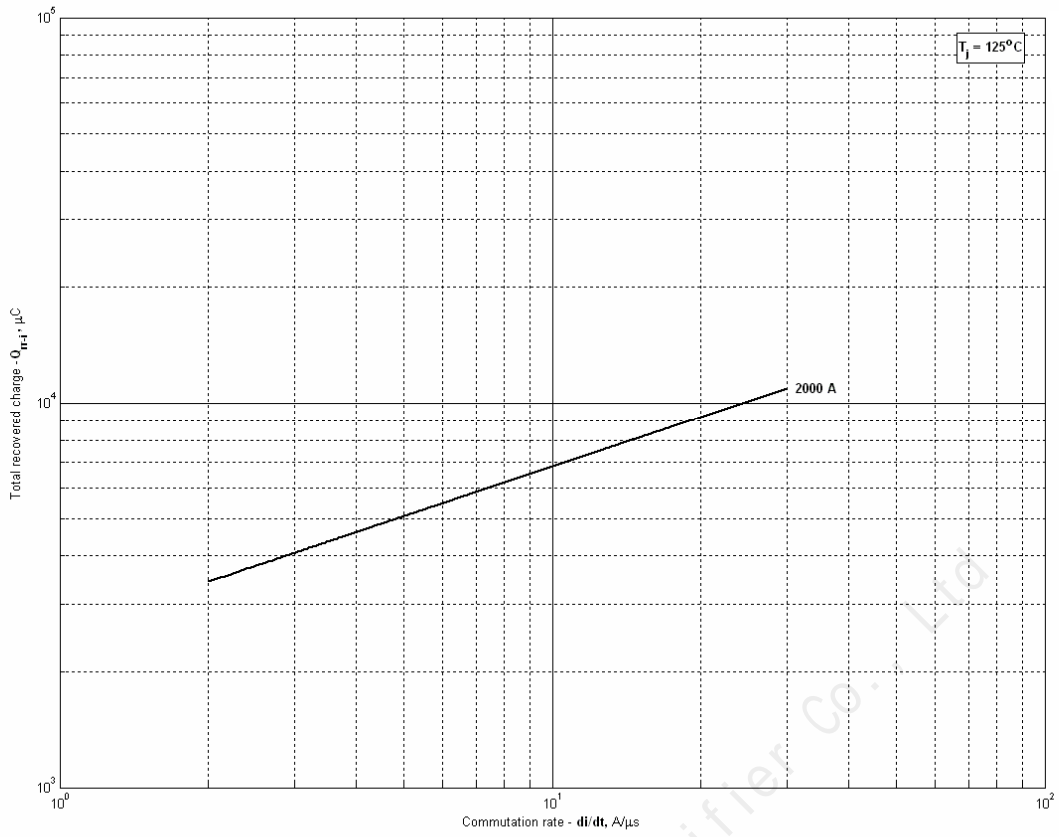


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

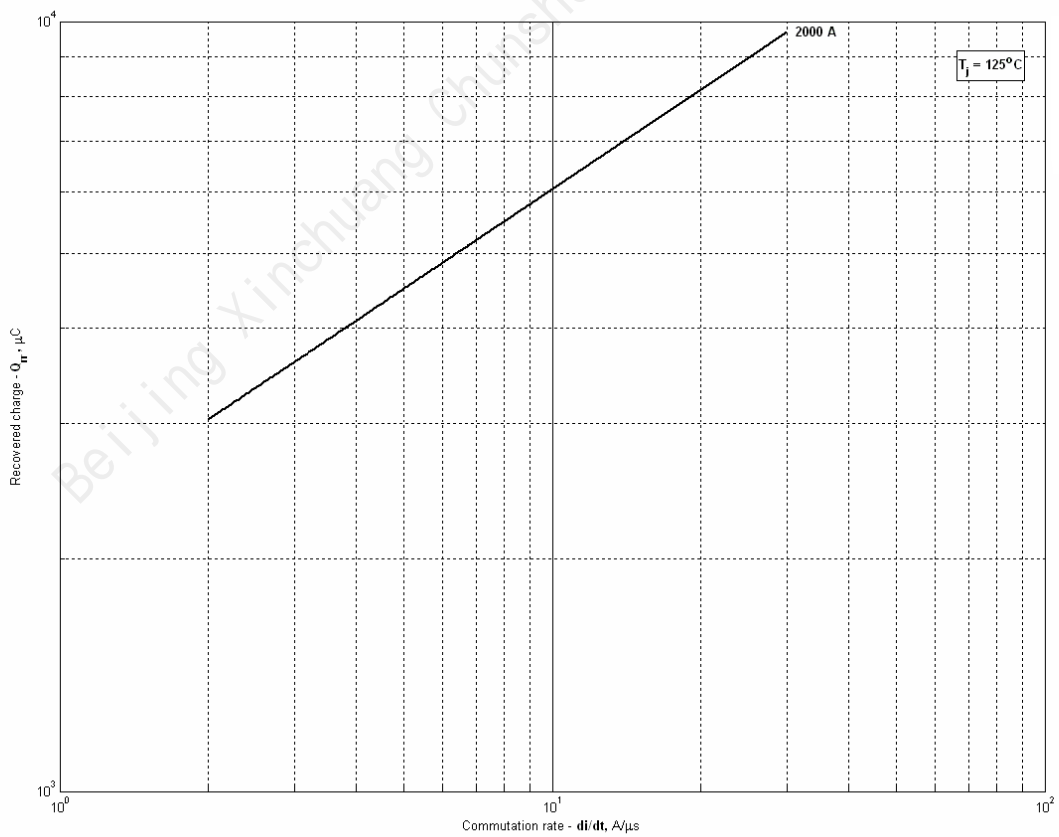


Fig 6 - Recovered charge, Q_{rr} (linear)

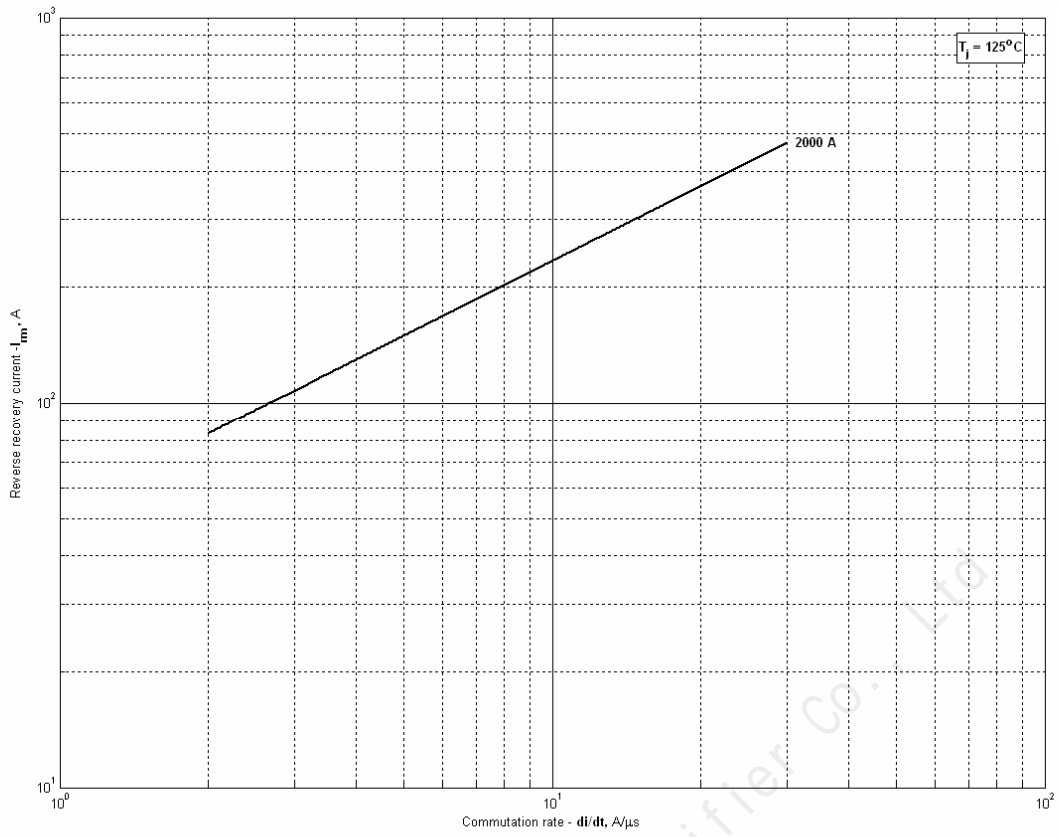


Fig 7 – Peak reverse recovery current, I_{rm}

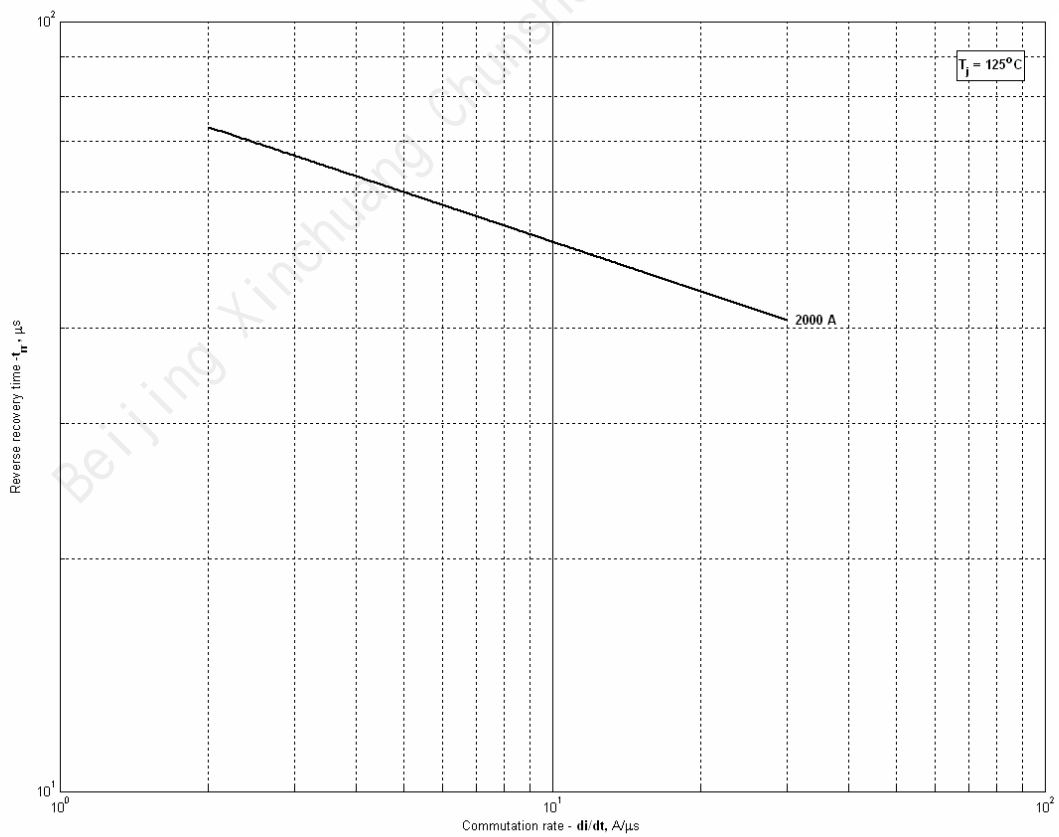


Fig 8 – Maximum recovery time, t_{rr} (linear)

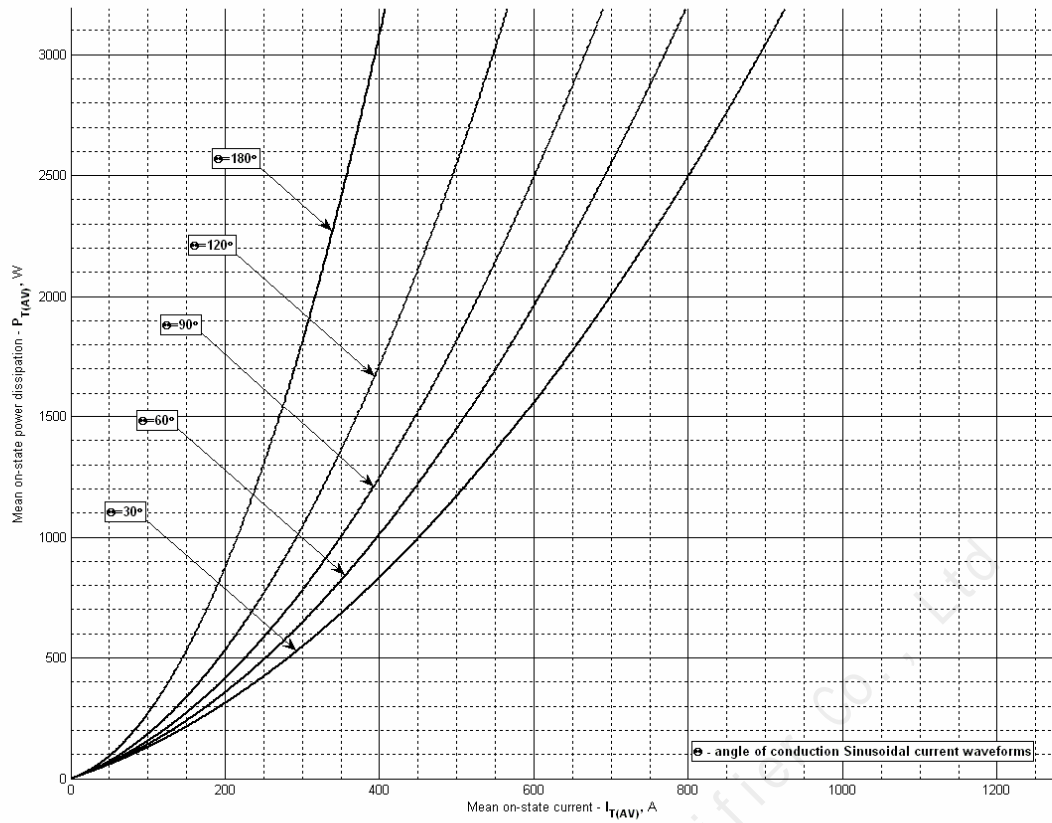


Fig 9 – On-state power loss (sinusoidal current waveforms)

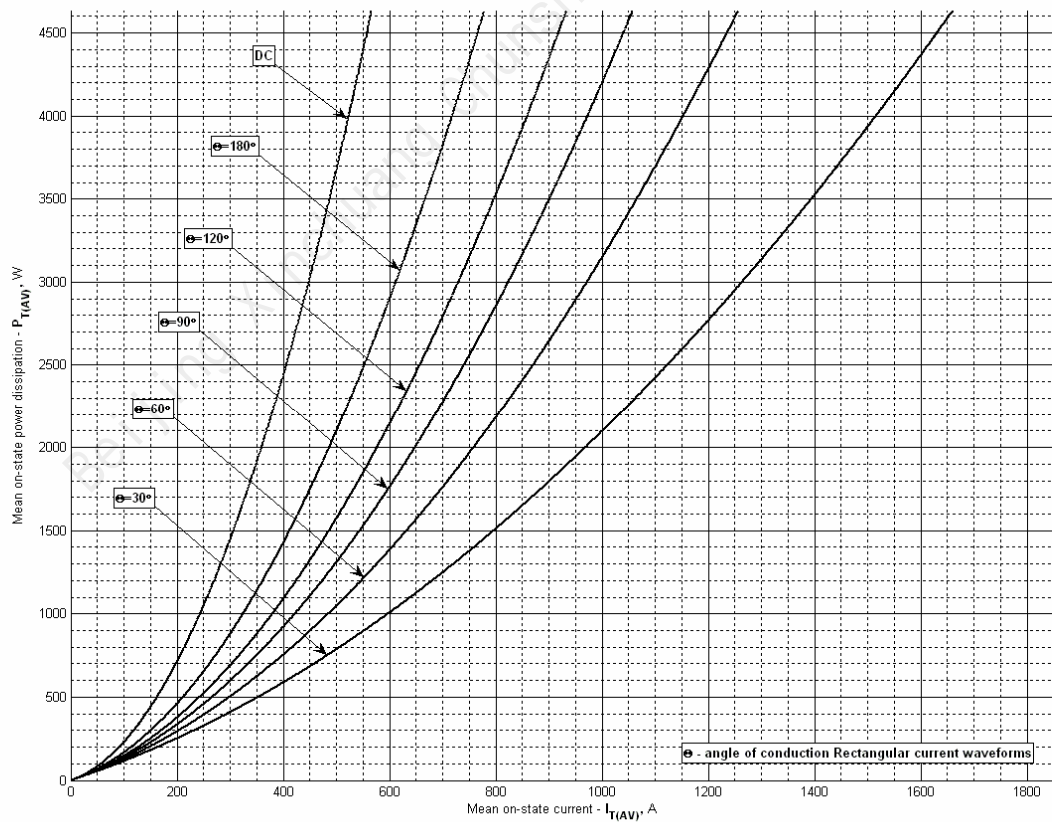


Fig 10 – On-state power loss (rectangular current waveforms)

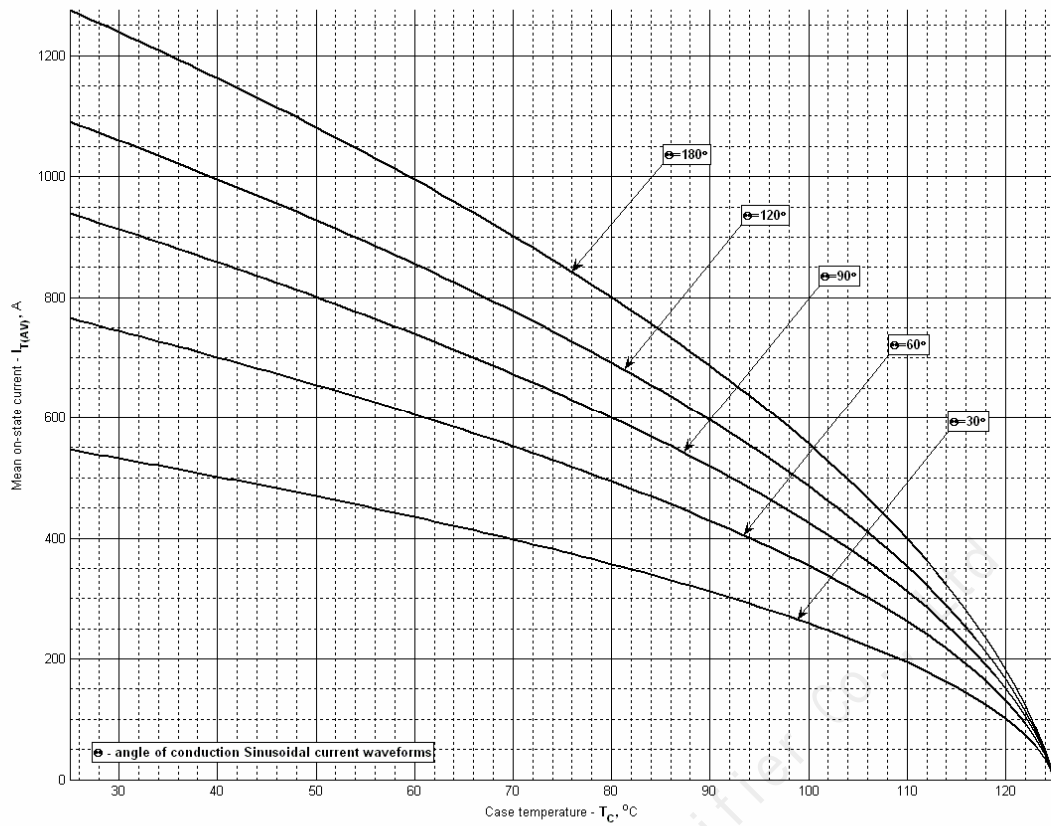


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

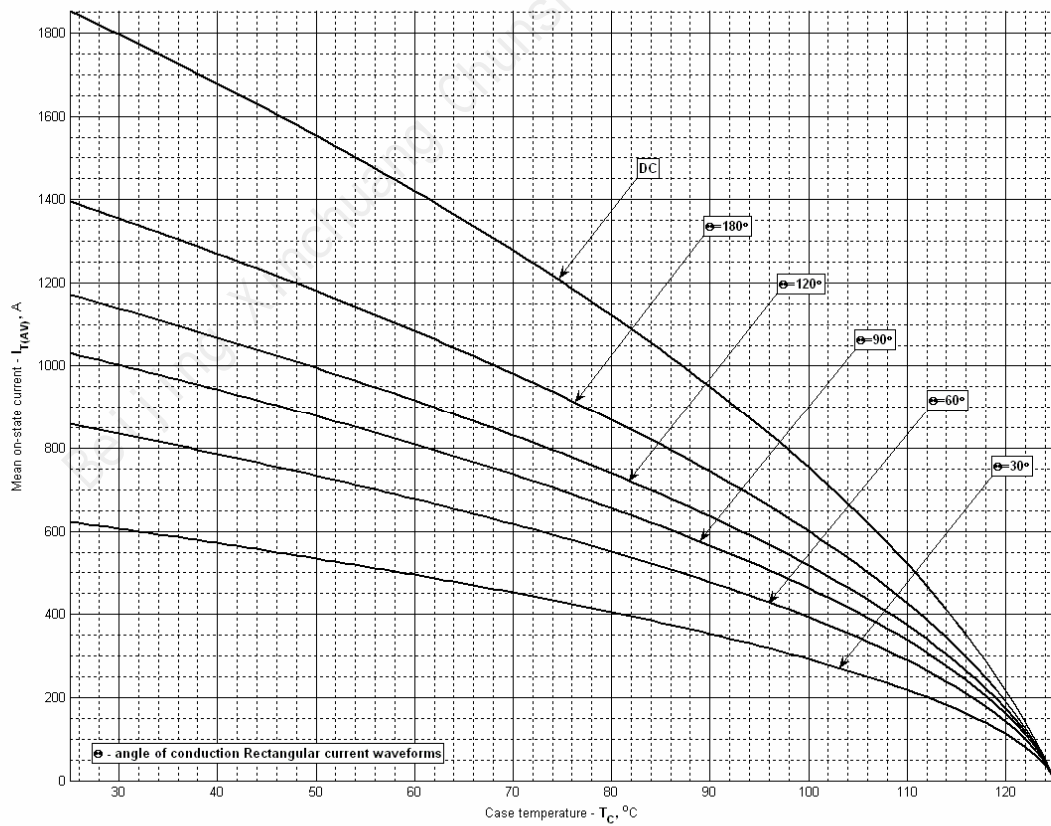


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

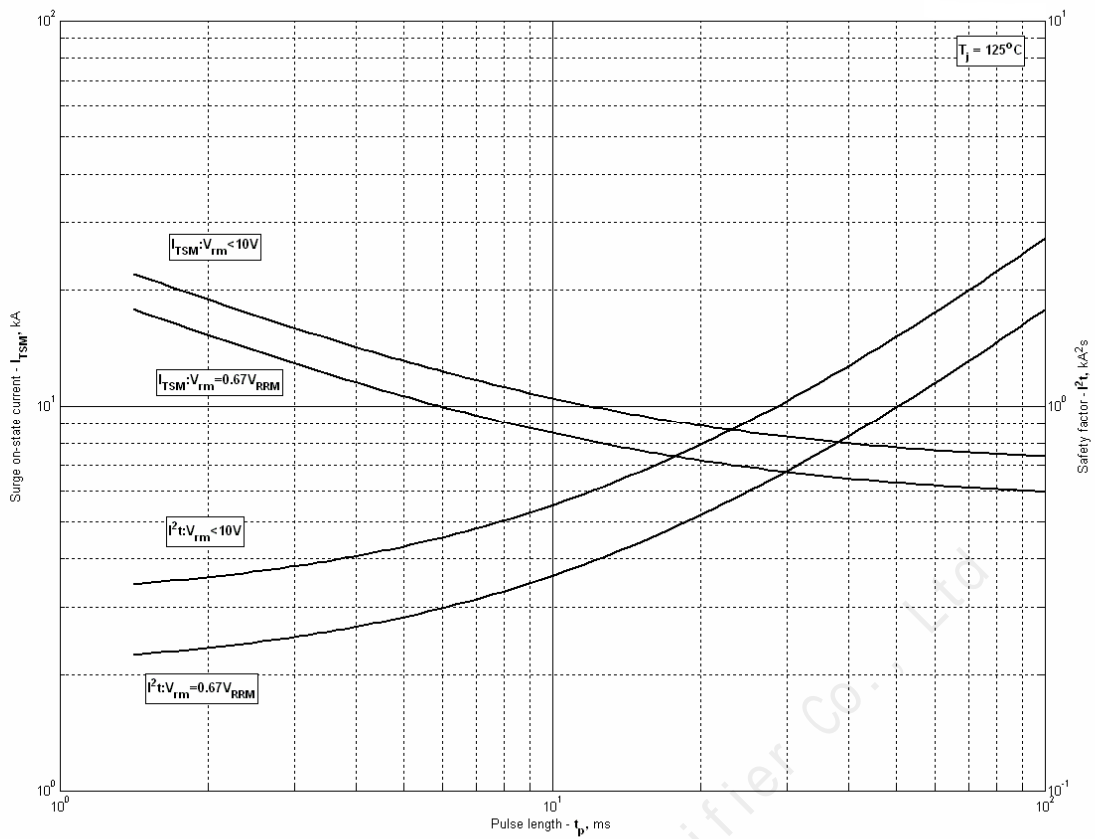


Fig 13 – Maximum surge and I^2t ratings

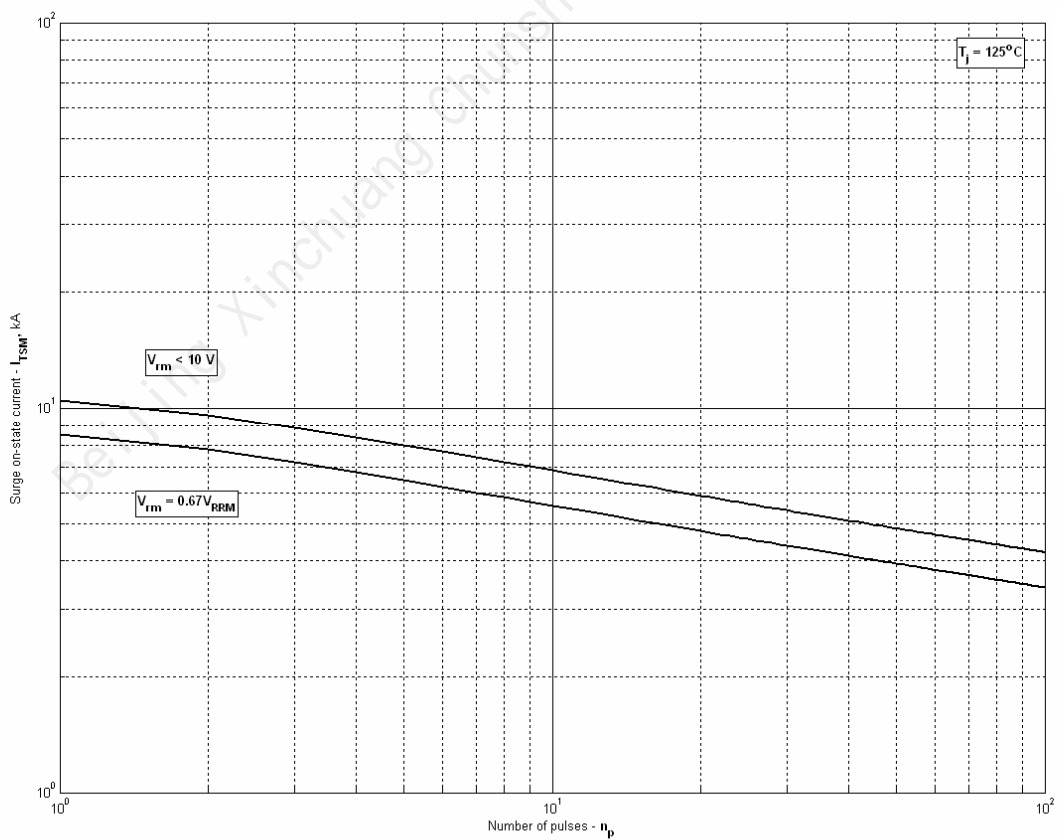


Fig 14 – Maximum surge ratings