ChunZheng

High-end Power Semiconductor Manufacturer

KP500A 4600V-6500V

Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current	I_{TAV}	500 A									
Repetitive peak off-state voltage	V_{DRM}	4600 — 6500 V									
Repetitive peak reverse voltage	V_{RRM}										
Turn-off time	t_q	800 μs									
V_{DRM}, V_{RRM}, V	4600	4800	5000	5200	5400	5600	5800	6000	6200	6400	6500
Voltage code	46	48	50	52	54	56	58	60	62	64	65
T_j, °C	-60 — 125										

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	500	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	785	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	9.5 11.0	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			10.0 11.5	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
I^2t	Safety factor	$A^2s·10^3$	450 600	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=10 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			410 540	T_j=$T_{j\ max}$ T_j=25 °C	180° half-sine wave; t_p=8.3 ms; single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600—6500	$T_{j\ min}$< T_j <$T_{j\ max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700—6600	$T_{j\ min}$< T_j <$T_{j\ max}$; 180° half-sine wave; single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	$0.6·V_{DRM}$ $0.6·V_{RRM}$	T_j=$T_{j\ max}$; Gate open	

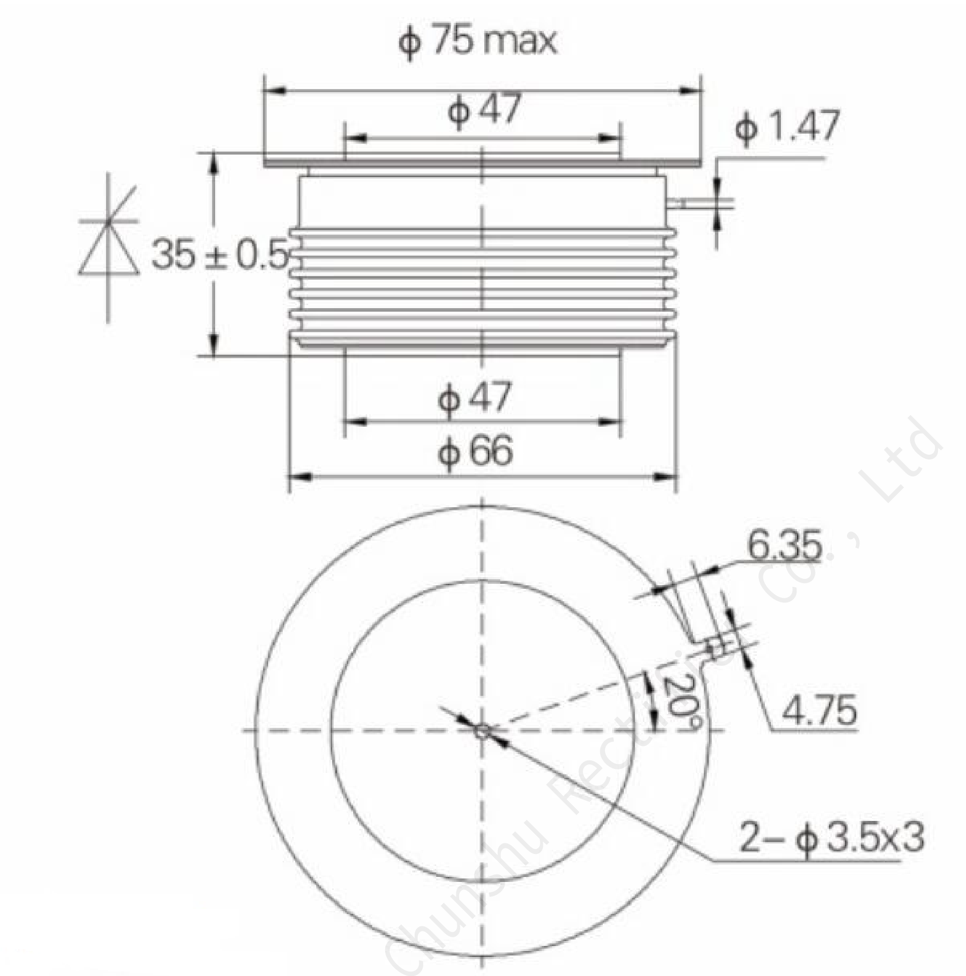
TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	$T_j=T_{j\,max}$
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/µs	400	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; I_{TM}=2150 A; Gate pulse: I_G=2 A; t_{GP}=50 µs; $di_G/dt \geq 2$ A/µs
THERMAL				
T_{stg}	Storage temperature	°C	-60−50	
T_j	Operating junction temperature	°C	-60−125	
MECHANICAL				
F	Mounting force	kN	24.0−28.0	
a	Acceleration	m/s^2	50	Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	2.70	T_j=25 °C; I_{TM}=1570 A
$V_{T(TO)}$	On-state threshold voltage, max	V	1.322	$T_j=T_{j\,max}$; $0.5\,\pi\,I_{TAV} < I_T < 1.5\,\pi\,I_{TAV}$
r_T	On-state slope resistance, max	mΩ	1.145	$T_j=T_{j\,max}$; $0.5\,\pi\,I_{TAV} < I_T < 1.5\,\pi\,I_{TAV}$
I_L	Latching current, max	mA	1500	T_j=25 °C; V_D=12 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; $di_G/dt \geq 1$ A/µs
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1], min	V/µs	1000, 1600, 2000, 2500	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	2.50 1.50	T_j=25 °C $T_j=T_{j\,max}$ V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 150	T_j= 25 °C $T_j=T_{j\,max}$ V_D=12 V; I_D=3 A; Direct gate current
V_{GD}	Gate non-trigger direct voltage, min	V	0.45	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current
I_{GD}	Gate non-trigger direct current, min	mA	65.00	$T_j=T_{j\,max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current
SWITCHING				
t_{gd}	Delay time, max	µs	3.00	T_j=25 °C; V_D=1500 V; $I_{TM}=I_{TAV}$; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs
t_{gt}	Turn-on time, max	µs	10.00	T_j=25 °C; V_D=1500 V; $I_{TM}=I_{TAV}$; di/dt=200 A/µs; Gate pulse: I_G=2 A; V_G=20 V; t_{GP}=50 µs; di_G/dt=2 A/µs
t_q	Turn-off time[2], max	µs	800	dv_D/dt=50 V/µs; $T_j=T_{j\,max}$; $I_{TM}=I_{TAV}$; di_R/dt=-10 A/µs; V_R=100V; V_D=2000 V
Q_{rr}	Total recovered charge, max	µC	4500	$T_j=T_{j\,max}$; I_{TM}=1000 A; di_R/dt=-5 A/µs; V_R=100 V
t_{rr}	Reverse recovery time, typ	µs	60.0	$T_j=T_{j\,max}$; I_{TM}=1000 A; di_R/dt=-5 A/µs; V_R=100 V
I_{rrM}	Peak reverse recovery current, max	A	150	$T_j=T_{j\,max}$; I_{TM}=1000 A; di_R/dt=-5 A/µs; V_R=100 V

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.020	Direct current	Double side cooled
R_{thjc-A}			0.044		Anode side cooled
R_{thjc-K}			0.036		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.004	Direct current	
MECHANICAL					
w	Weight, max	g	700		
D_s	Surface creepage distance	mm (inch)	39.55 (1.557)		
D_a	Air strike distance	mm (inch)	25.50 (1.004)		

OVERALL DIMENSIONS



KT55DT

All dimensions in millimeters

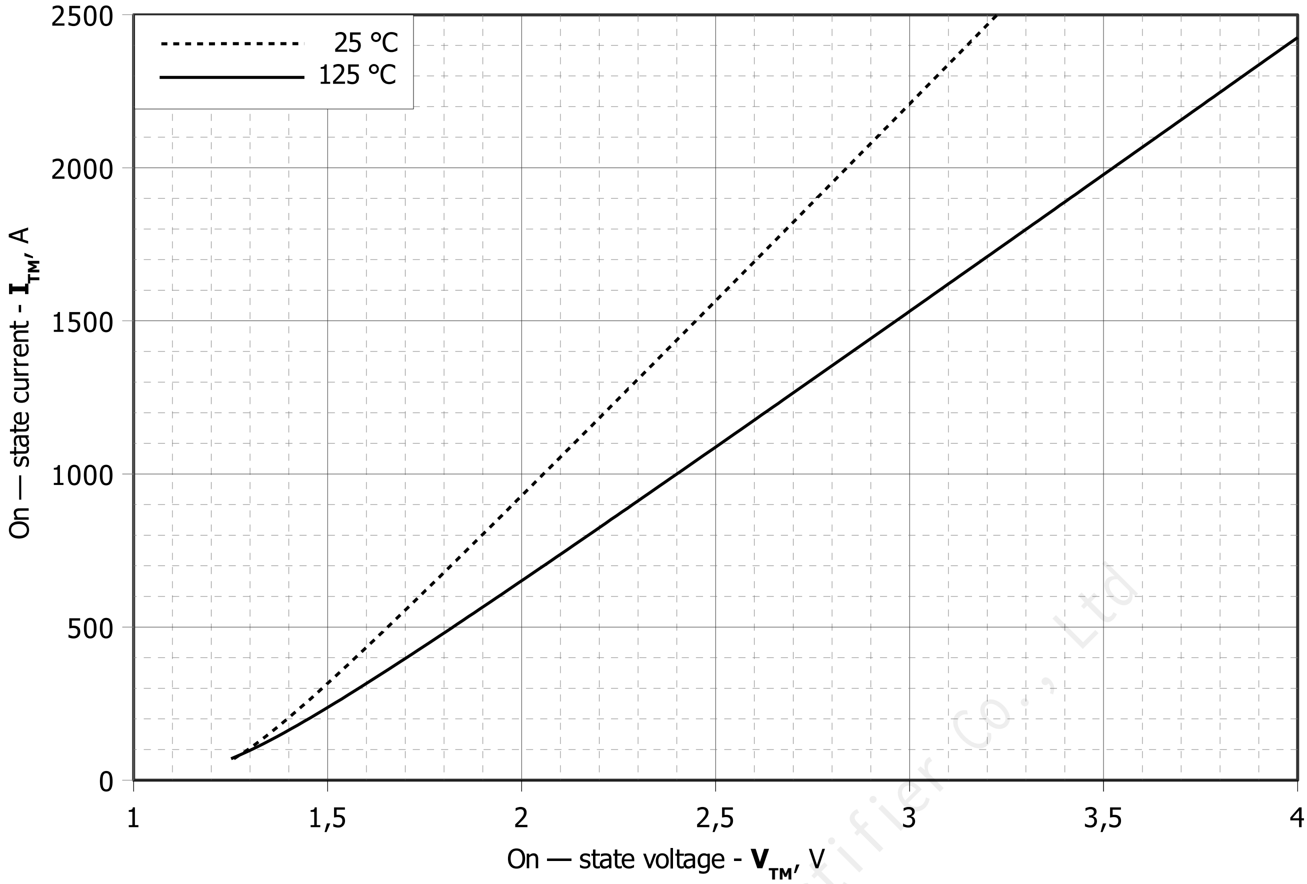


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	$T_j = T_{j\,max}$
A	1.02180000	0.89838310
B	0.00077615	0.00112210
C	0.04676500	0.07137240
D	-0.00204380	-0.00358350

On-state characteristic model (see Fig. 1)

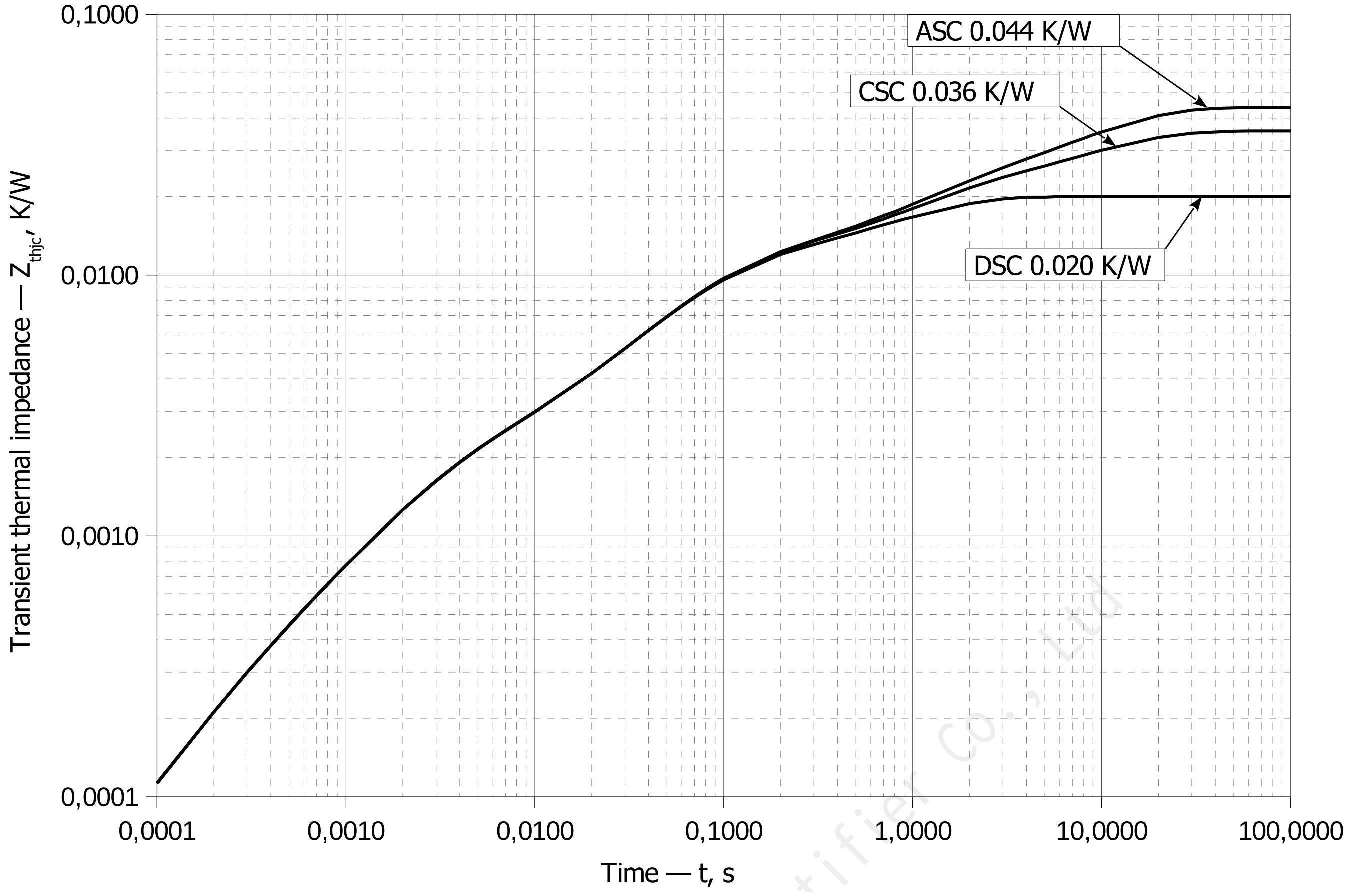


Fig 2 – Transient thermal impedance Z_{thjc} vs. time t

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t.

R_i = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i, K/W	0.009168	0.002899	0.001522	0.006297	0.00003033	0.00008163
τ_i, s	0.9681	0.05144	0.002417	0.07706	0.0004122	0.0002166

DC Anode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.02398	0.009274	0.009094	-0.00003741	0.00155	0.0001282
τ_i, s	9.752	1.065	0.06762	0.01374	0.002533	0.0002841

DC Cathode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.01568	0.00922	0.009098	0.00006319	0.001526	0.000116
τ_i, s	9.755	1.039	0.06857	0.01397	0.002449	0.0002632

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

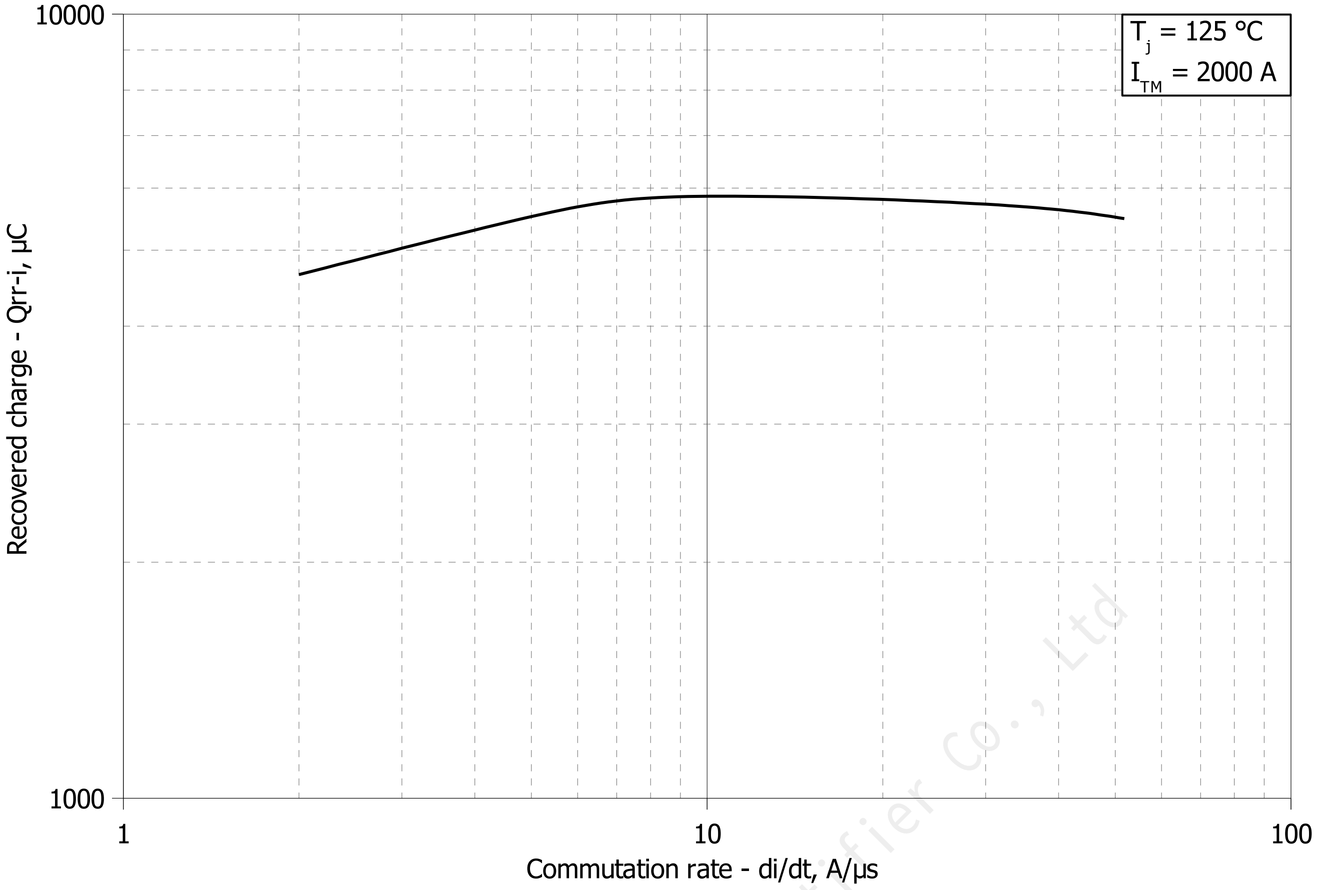


Fig 3 – Maximum recovered charge Q_{rr-i} (integral) vs. commutation rate di_R/dt

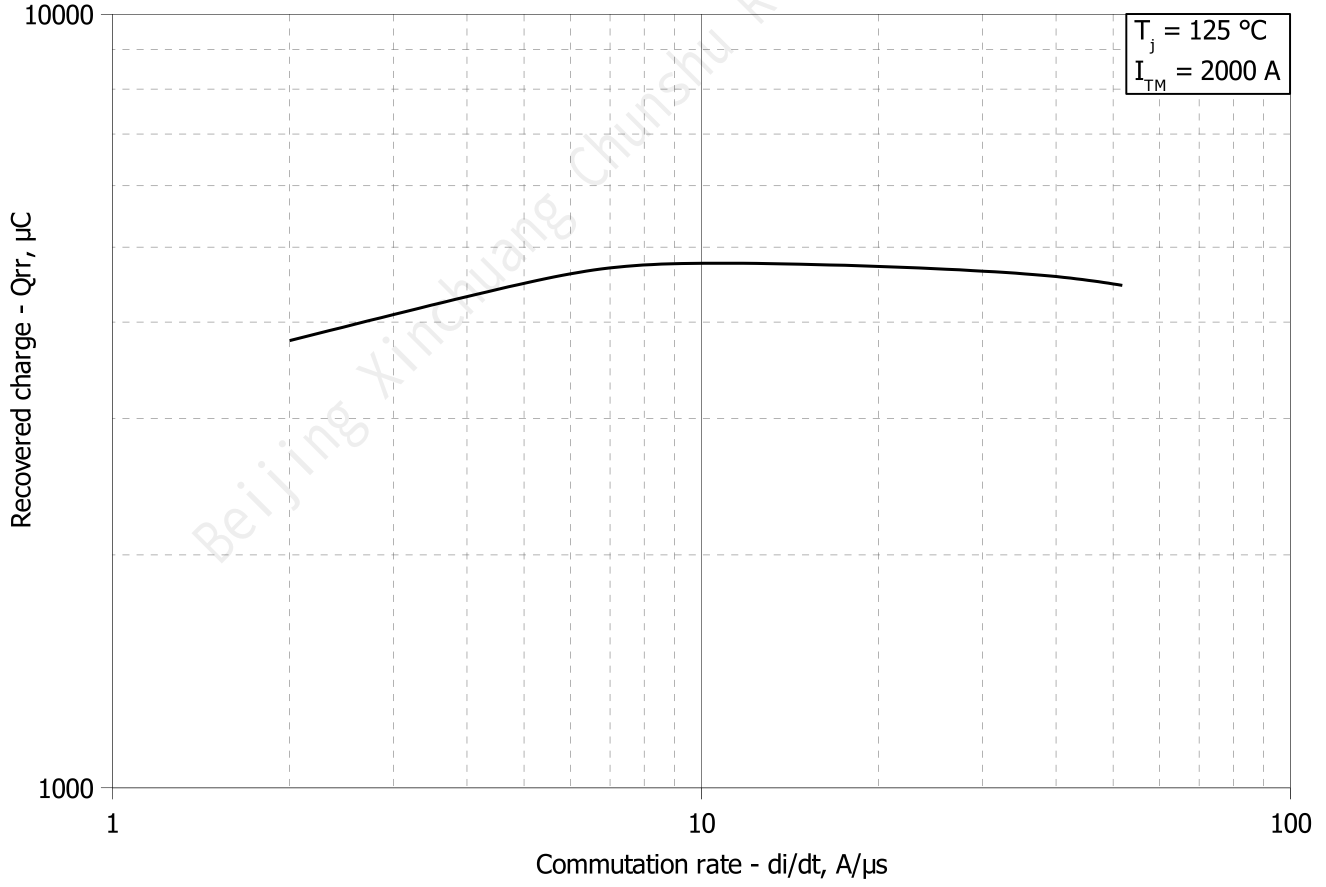


Fig 4 – Maximum recovered charge Q_{rr} vs. commutation rate di_R/dt (25% chord)

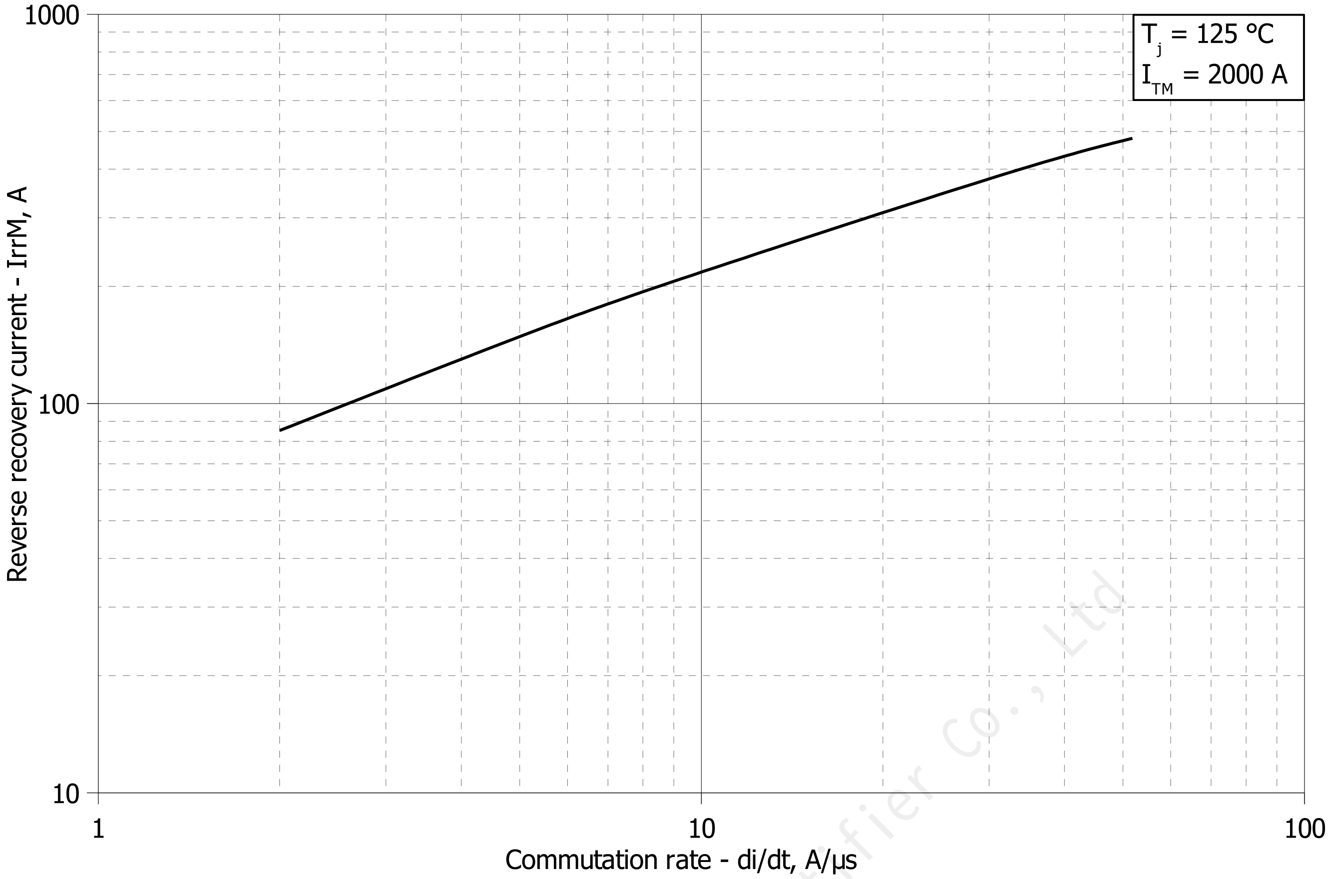


Fig 5 – Maximum reverse recovery current I_{rrM} vs. commutation rate di_R/dt

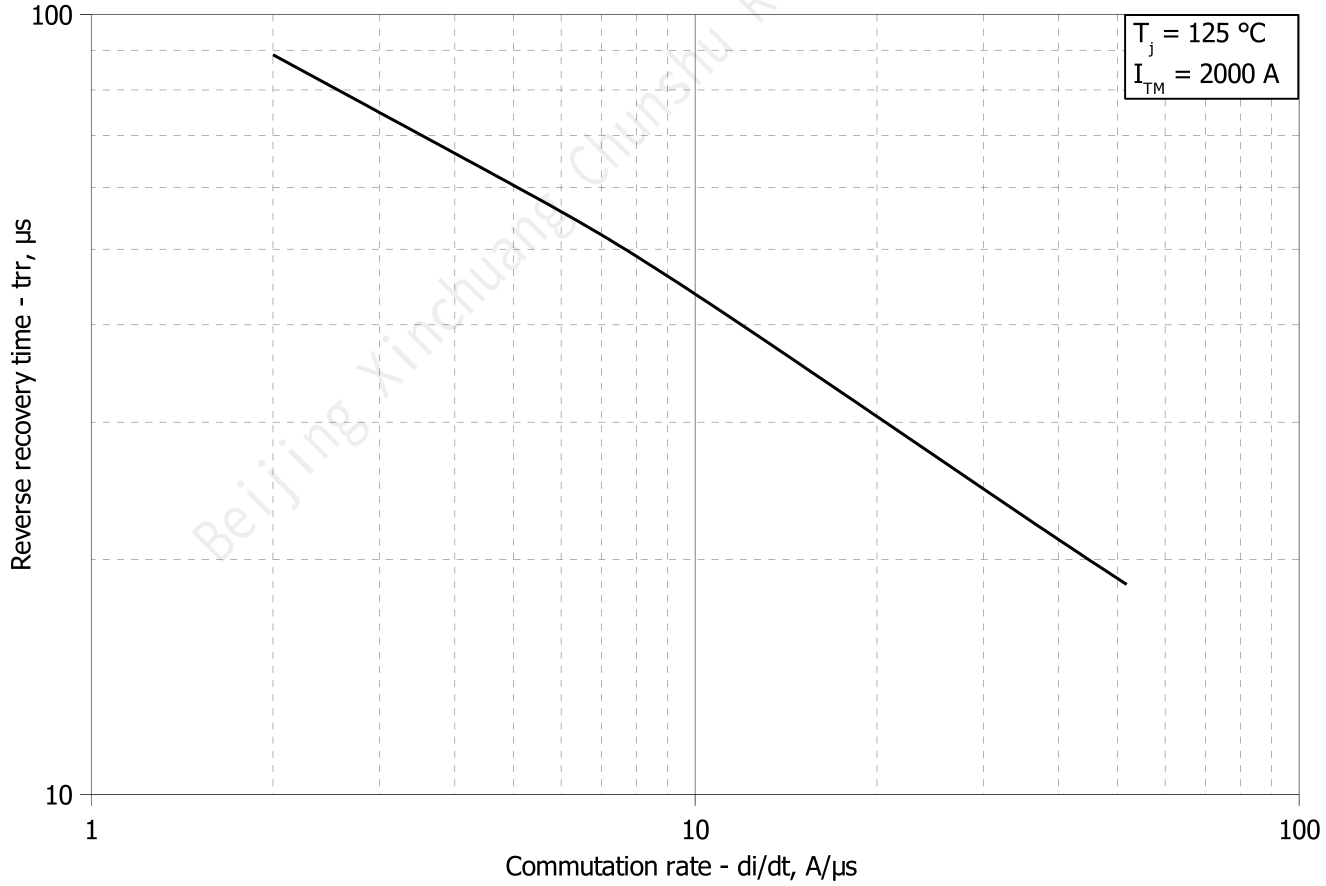


Fig 6 – Maximum recovery time t_{rr} vs. commutation rate di_R/dt (25% chord)

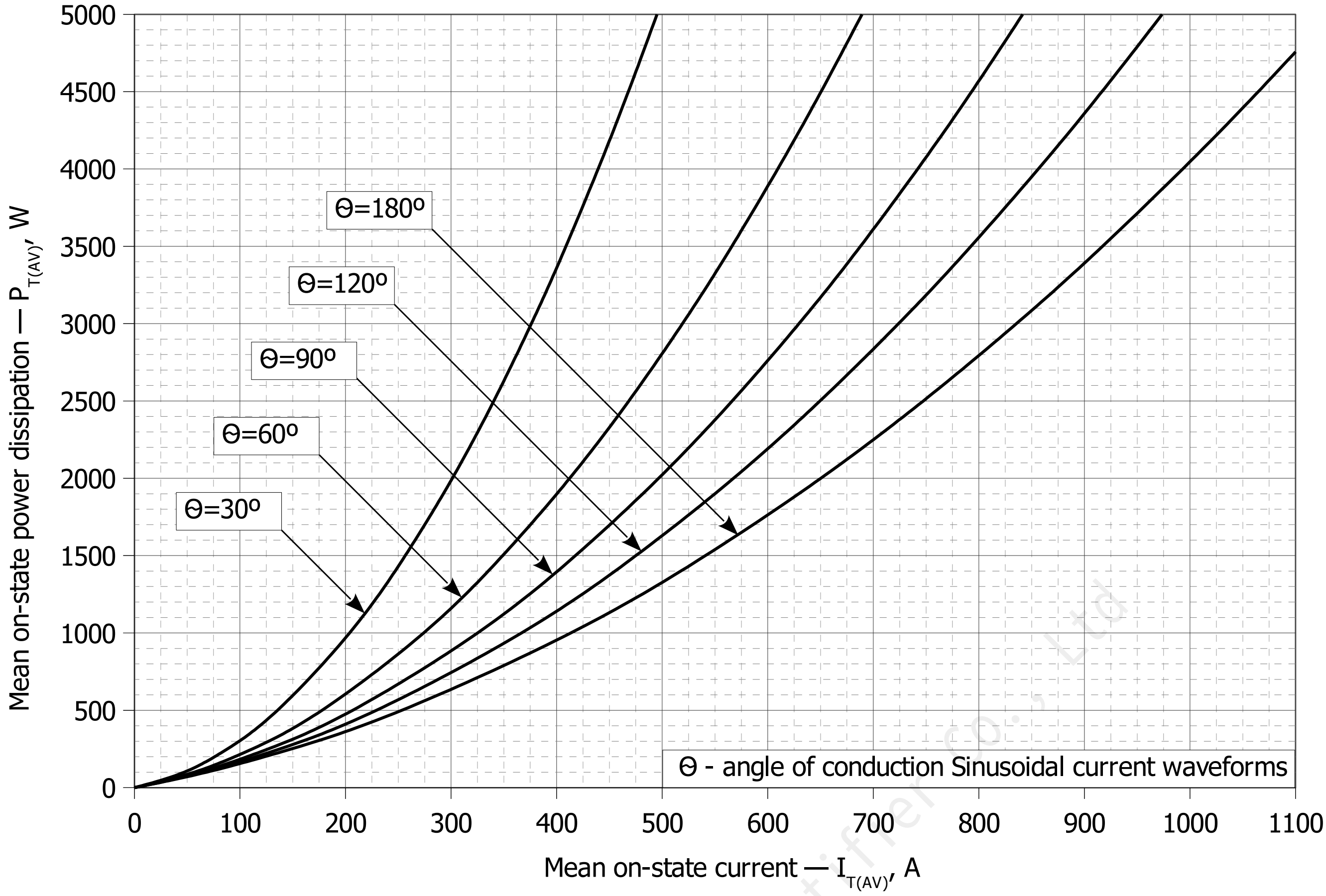


Fig. 7 - Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

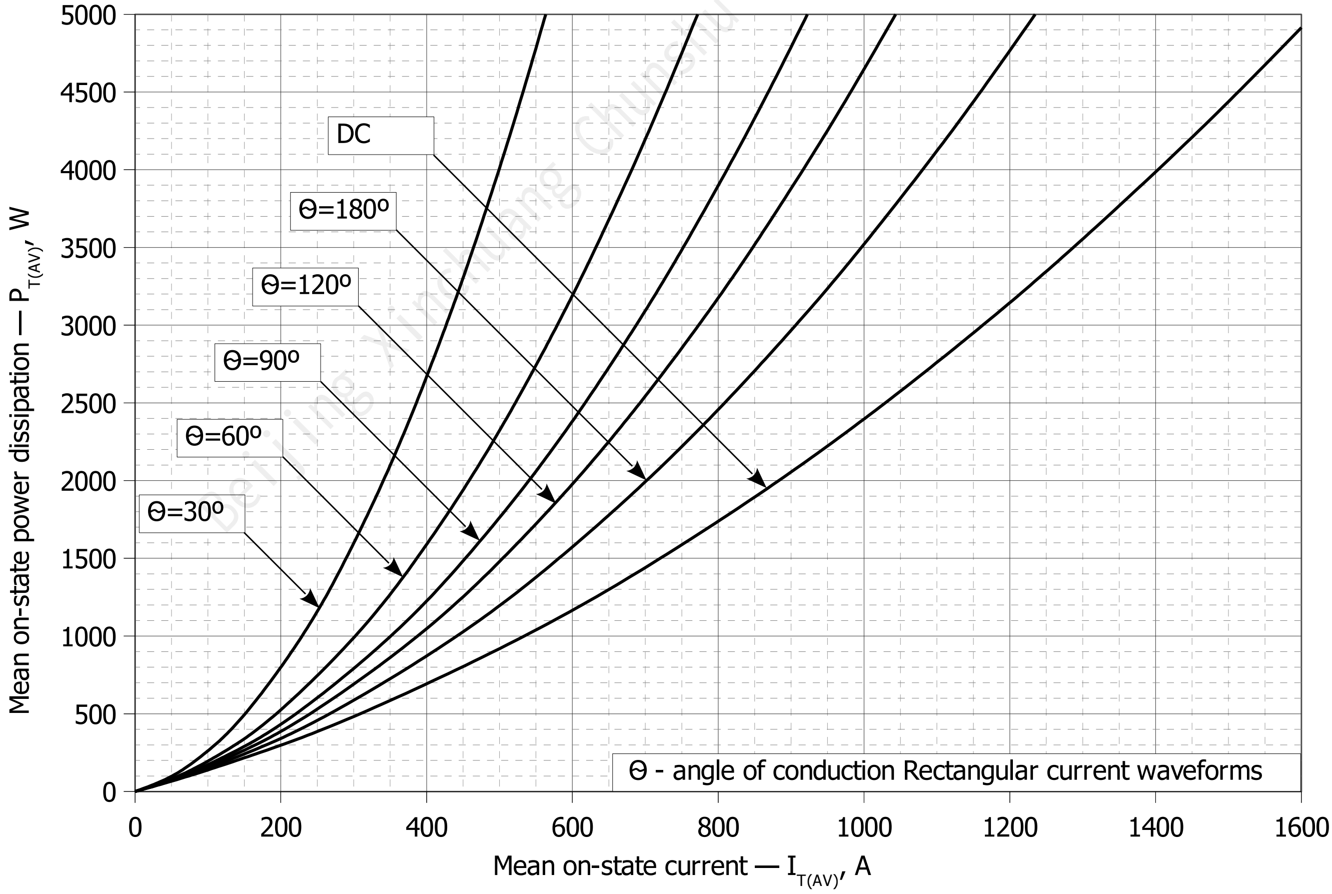


Fig. 8 – Mean on-state power dissipation P_{TAV} vs. mean on-state current I_{TAV} for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

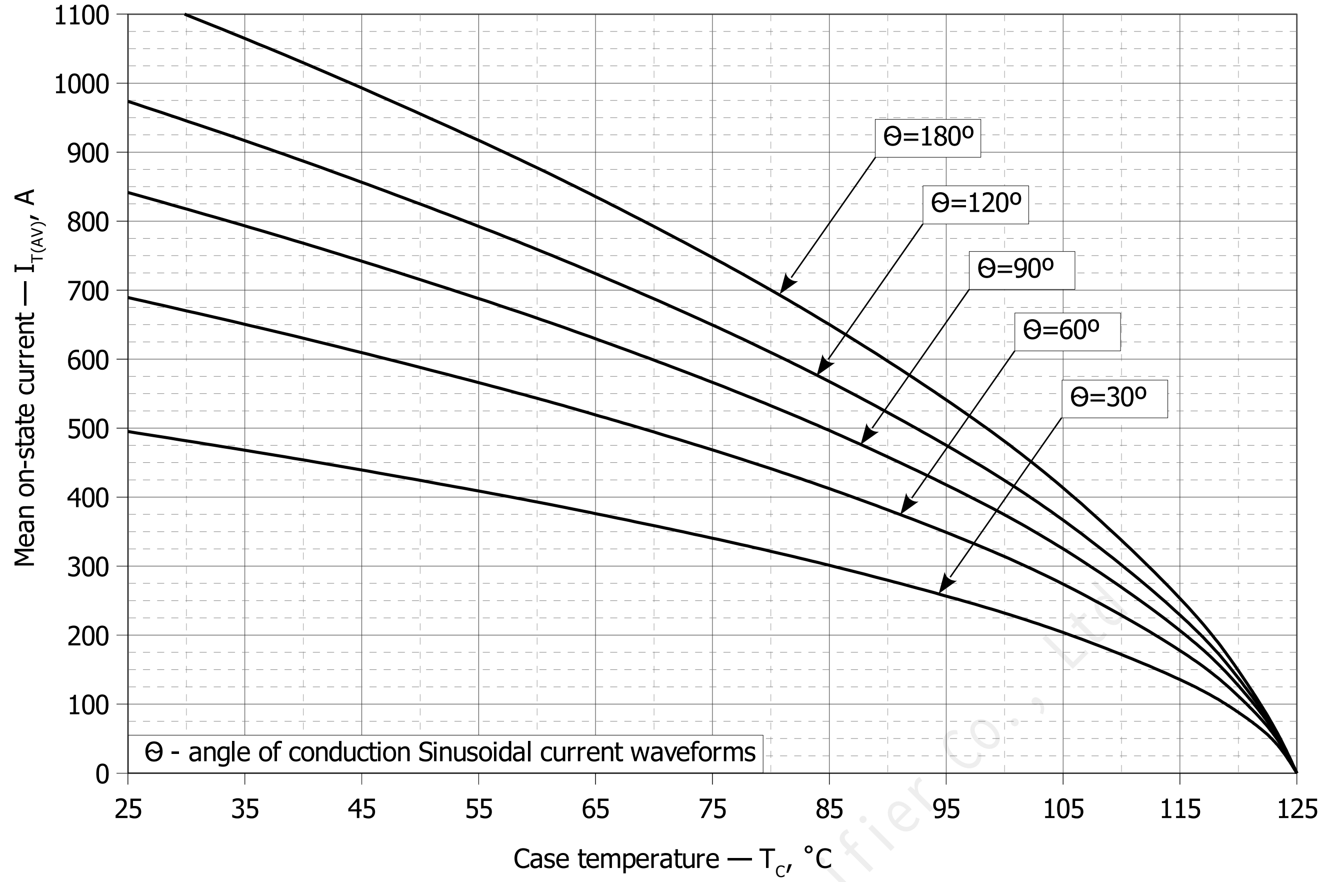


Fig. 9 – Mean on-state current I_{TAV} vs. case temperature T_C for sinusoidal current waveforms at different conduction angles (f=50Hz, DSC)

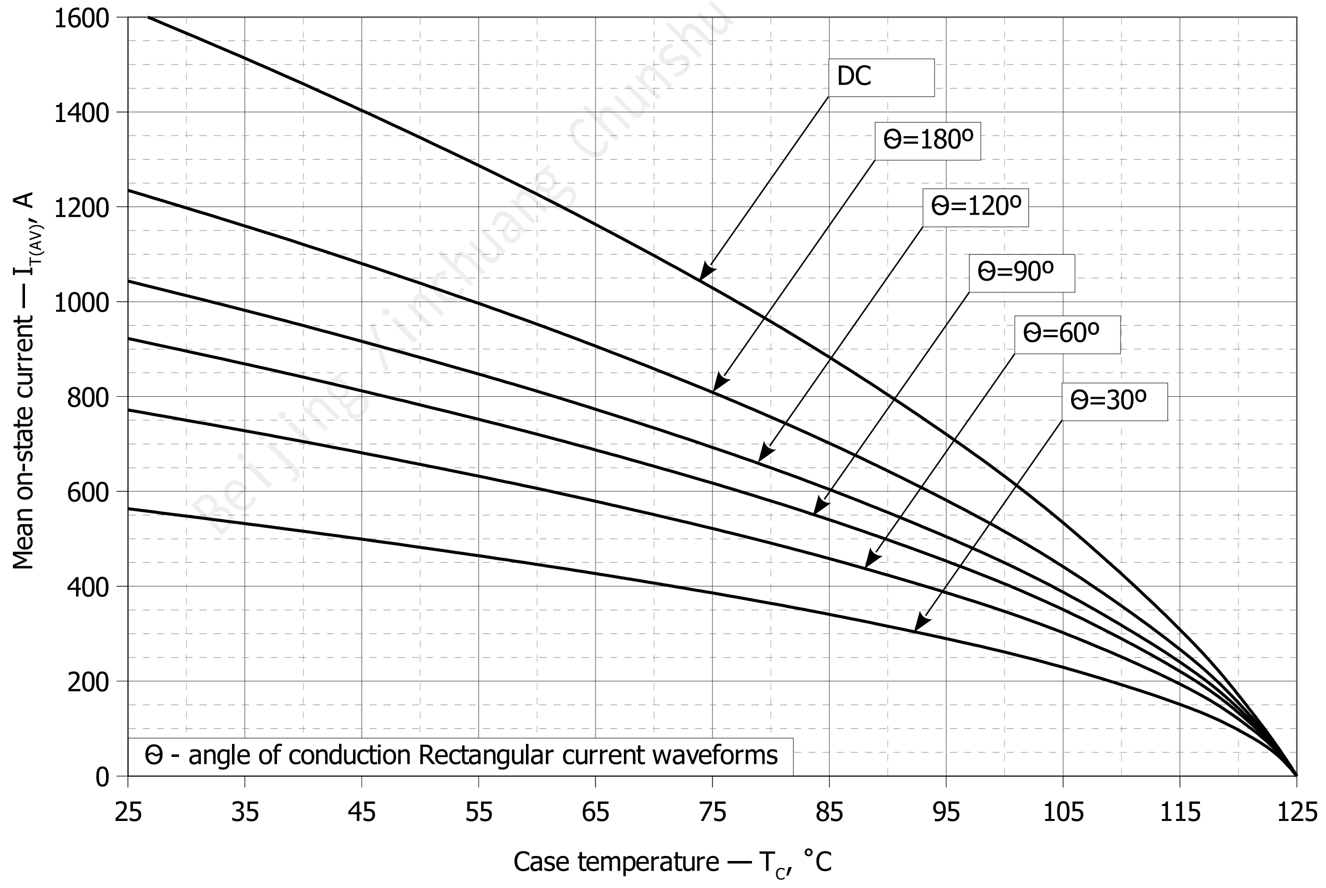


Fig. 10 - Mean on-state current I_{TAV} vs. case temperature T_C for rectangular current waveforms at different conduction angles and for DC (f=50Hz, DSC)

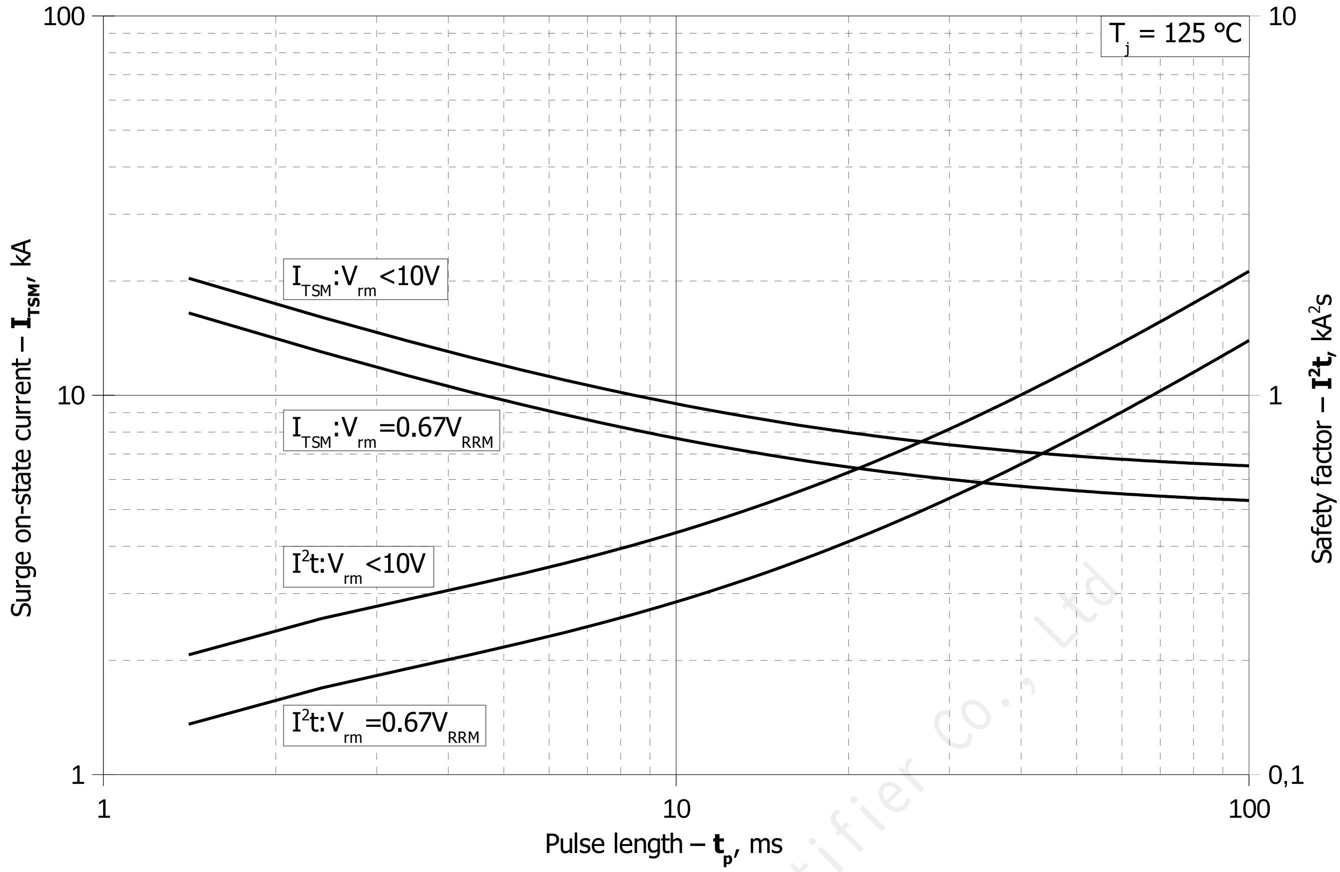


Fig. 11 – Maximum surge on-state current I_{TSM} and safety factor I^2t vs. pulse length t_p

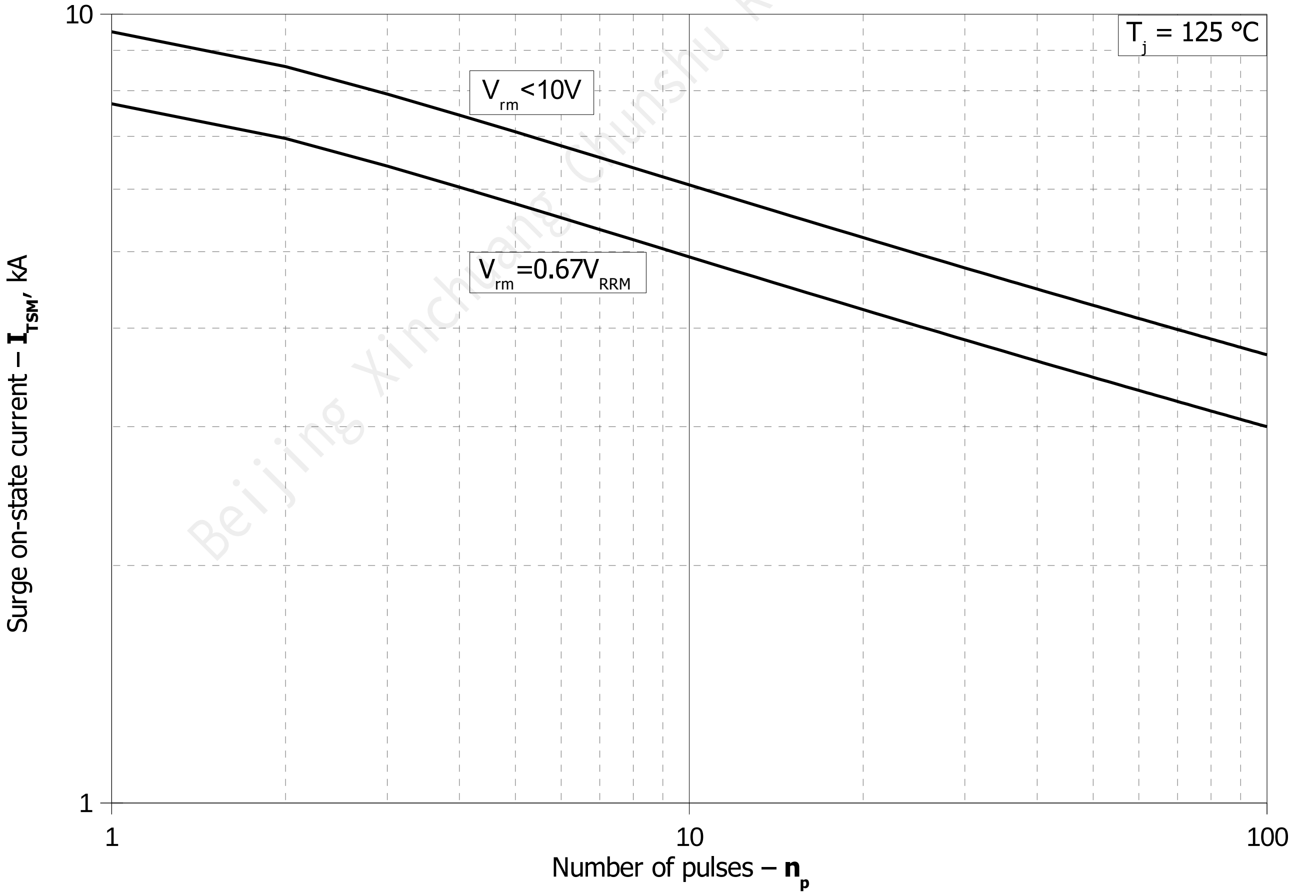


Fig. 12 - Maximum surge on-state current I_{TSM} vs. number of pulses n_p