ChunZheng

High-end Power Semiconductor Manufacturer

KP500A 7600V-8000V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current			I_{TAV}	500 A	
Repetitive peak off-state voltage			V_{DRM}	7600 −8000 V	
Repetitive peak reverse voltage			V_{RRM}		
Turn-off time			t_q	1200 μs	
V_{DRM}, V_{RRM}, V	7600	7700	7800	7900	8000
Voltage code	76	77	78	79	80
T_j, °C	-40 – 115				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	500	T_c=70 °C; 180° half-sine wave;	
I_{TRMS}	RMS on-state current	A	785	T_c=70 °C	
I_{TSM}	Surge on-state current	kA	12.1	T_j=$T_{j\,max}$	180° half-sine wave; (t_p=10 ms); V_R=0 V;
I^2t	Safety factor	$A^2s{\cdot}10^4$	73.2		180° sine wave; (t_p=10 ms);
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	7600-8000	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	8100-8500	T_{vj} = 25, 115 ° C; I_{DRM}, I_{RRM}≤200 mA; V_{DM} = V_{DRM}; V_{RM} = V_{RRM}; t_p= 10 ms; Gate open	

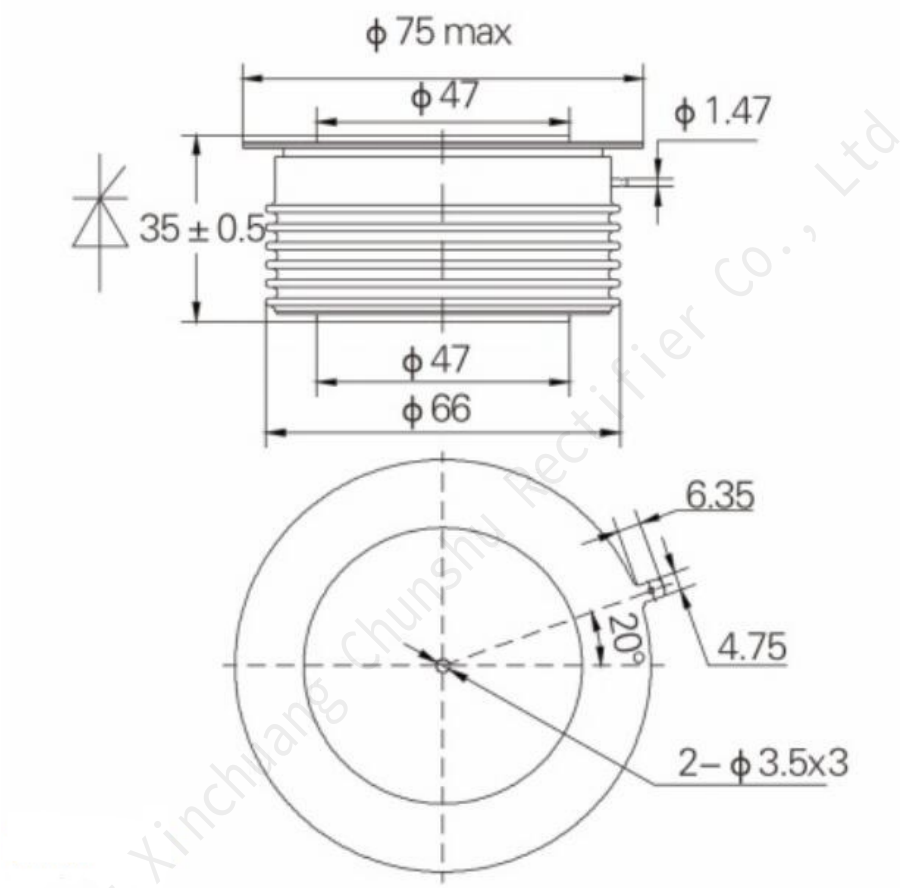
TRIGGERING				
I_{FGM}	Peak forward gate current	A	4	
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	20	
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive	A/μs	100	T_{vj} = 115°C; V_{DM} = 0.67 V_{DRM}; f = 50 Hz; I_{TM} = 600 A; I_{FG} = 2 A; t_r= 0.5 μs
THERMAL				
Tstg	Storage temperature	°C	-40-140	
T_j	Operating junction temperature	°C	-40-115	
MECHANICAL				
F	Mounting force	kN	22.0	

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions
ON-STATE				
V_{TM}	Peak on-state voltage, max	V	2.90	T_j=115 °C; I_{TM}=1000 A
$V_{T(TO)}$	On-state threshold voltage, max	V	1.35	T_j=$T_{j\,max}$
r_T	On-state slope resistance, max	mΩ	1.550	
I_L	Latching current, max	mA	1000	T_j=25 °C
I_H	Holding current, max	mA	200	T_j=25 °C
BLOCKING				
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	T_j=25 °C, 115 °C; V_{DRM}/V_{RRM}; Gate open
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	2000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open
TRIGGERING				
V_{GT}	Gate trigger direct voltage, max	V	3.00	T_j=25 °C
I_{GT}	Gate trigger direct current, max	mA	300	T_j= 25 °C
V_{GD}	Gate non-trigger direct voltage, min	V	0.30	T_j=$T_{j\,max}$; V_D=0.4·V_{DRM};
SWITCHING				
t_q	Turn-off time[2)], max	μs	1200	T_{vj} = 115°C; V_{DM} = 0.67 V_{DRM}; I_T =1000 A; dv/dt = 20 V/μs; V_R = 200 V; -di/dt = 1.5 A/μs
Q_{rr}	Total recovered charge, max	μC	3500	T_{vj} = 115 °C; -di /dt = 1.5 A/μs; I_T =1000 A; V_R = 200 V
I_{rrM}	Peak reverse recovery current, max	mA	200	T_{vj} = 25 °C, 115 °C; V_{DRM}/V_{RRM} Gate open

THERMAL				
R_{thjc}	Thermal resistance, junction to case, max	◦C/W	0.022	Direct current
R_{thck}	Thermal resistance, case to heatsink, max	◦C/W	0.005	Direct current
MECHANICAL				
w	Weight, typ	g	470	

OVERALL DIMENSIONS



KT55DT

All dimensions in millimeters

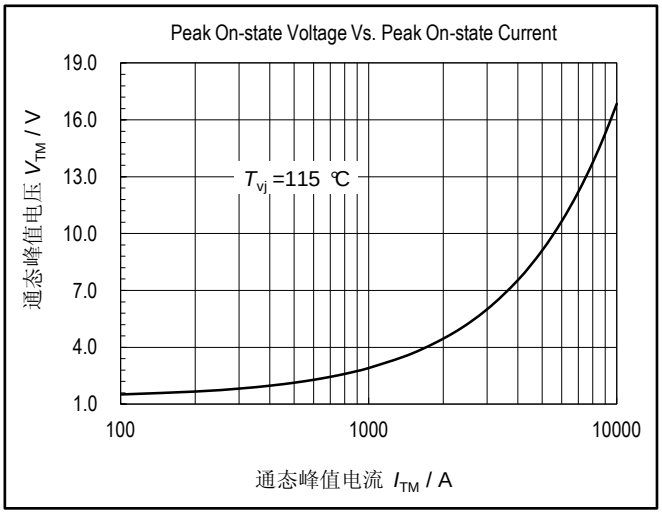


图1. 通态伏安特性曲线

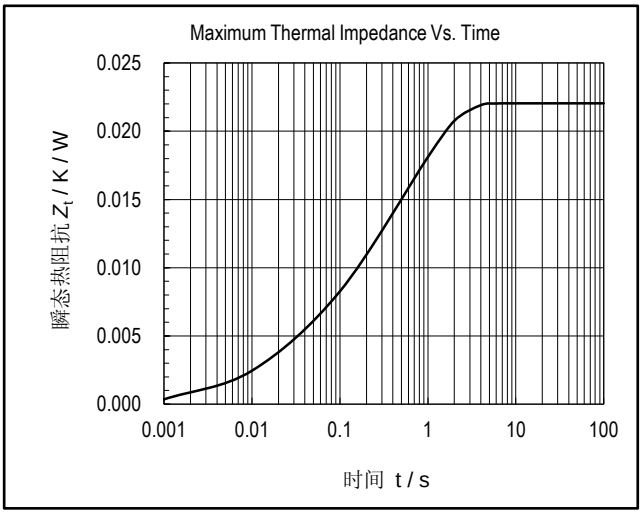


图2. 瞬态热阻抗曲线

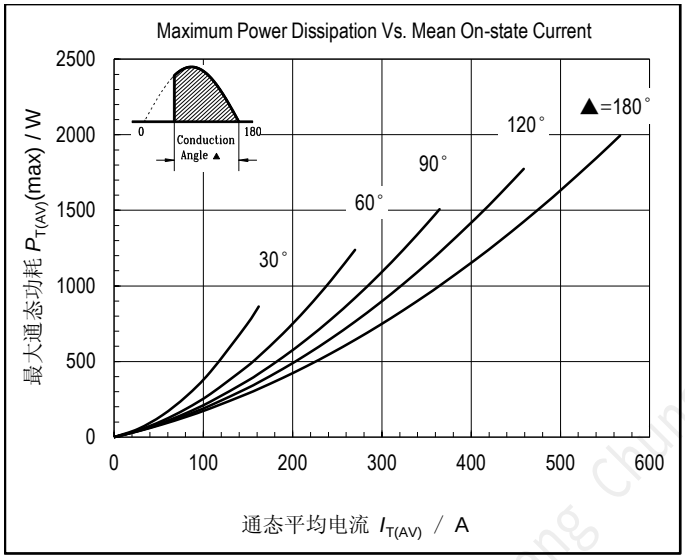


图3. 最大功耗与通态平均电流的关系曲线

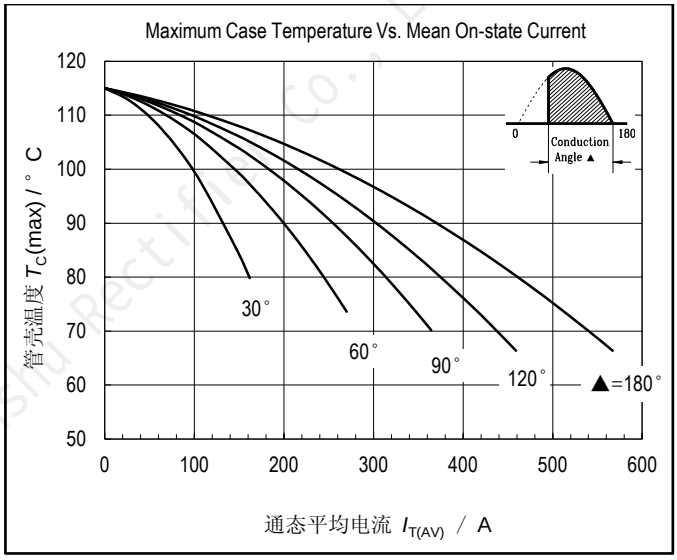


图4. 管壳温度与通态平均电流的关系曲线

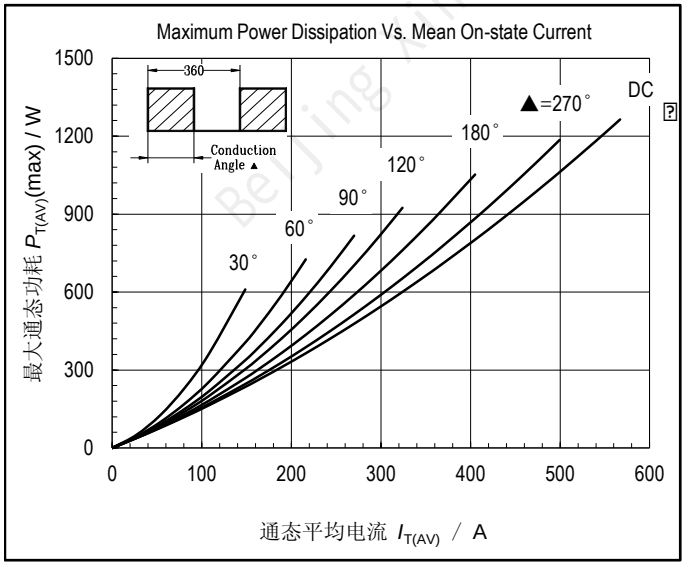


图5. 最大通态功耗与通态平均电流的关系曲线

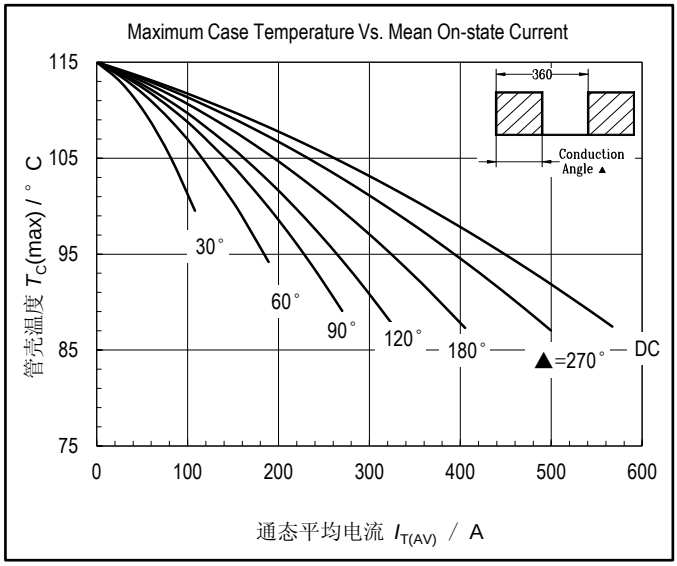


图6. 管壳温度与通态平均电流的关系曲线

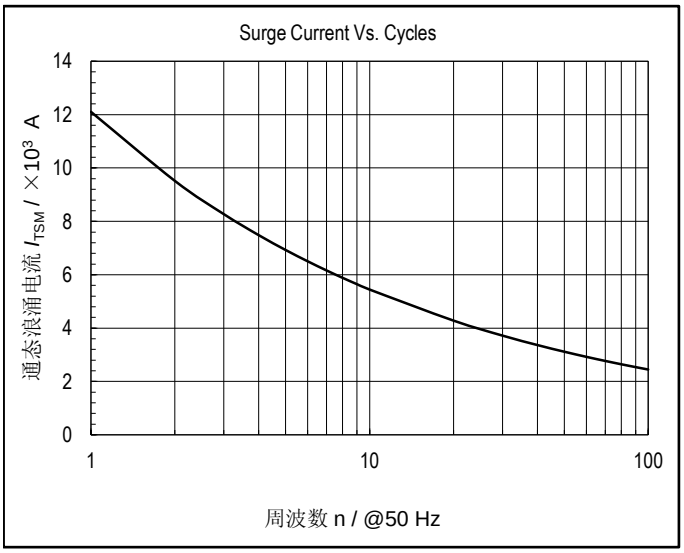


图7. 通态浪涌电流与周波数的关系曲线

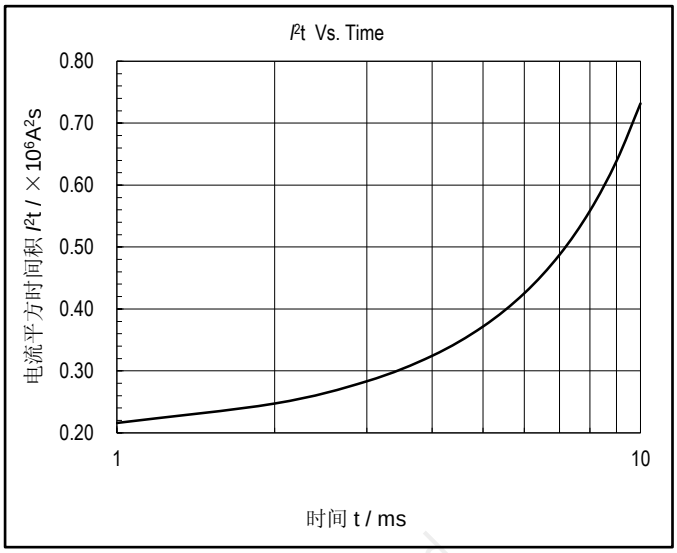


图8. I^2t 特 性 曲 线

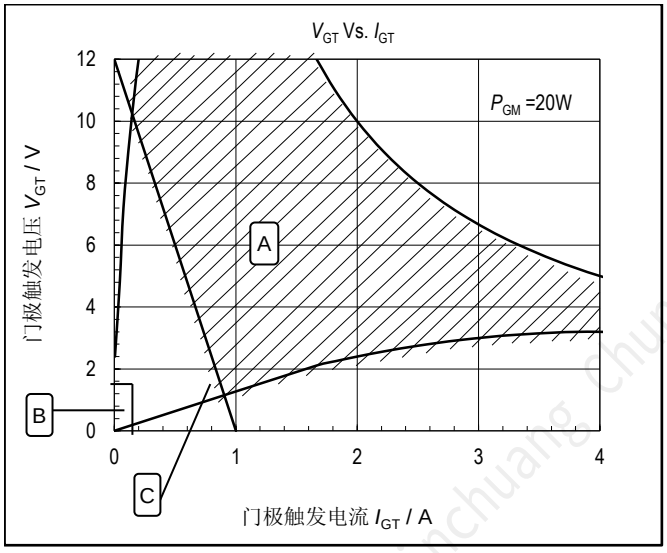


图9. 门极触发特性曲线

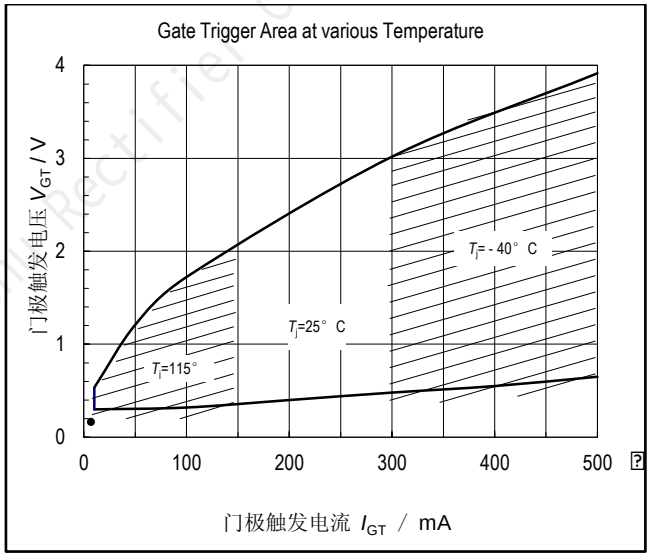


图10. 不同结温下的门极触发区

A为可靠触发区，
B为不可靠触发区。
C为建议采用的门极负载线。

A is Recommended Triggering Area.
B is Unreliable Triggering Area.
C is Recommended Gate Load Line.