ChunZheng

High-end Power Semiconductor Manufacturer

KP400A 1000V-1800V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current			I_{TAV}	400 A	
Repetitive peak off-state voltage			V_{DRM}	1000 – 1800 V	
Repetitive peak reverse voltage			V_{RRM}		
Turn-off time			t_q	125 μs	
V_{DRM}, V_{RRM}, V	1000	1200	1400	1600	1800
Voltage code	10	12	14	16	18
T_j, °C	-60 – 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	400	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	628	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	8.0 9.2	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			8.4 9.7	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
I^2t	Safety factor	A^2s	0.126×10^6	T_j=$T_{j\,max}$	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_R=0.67·V_{RRM}; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			0.320×10^6 0.423×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			0.293×10^6 0.387×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs

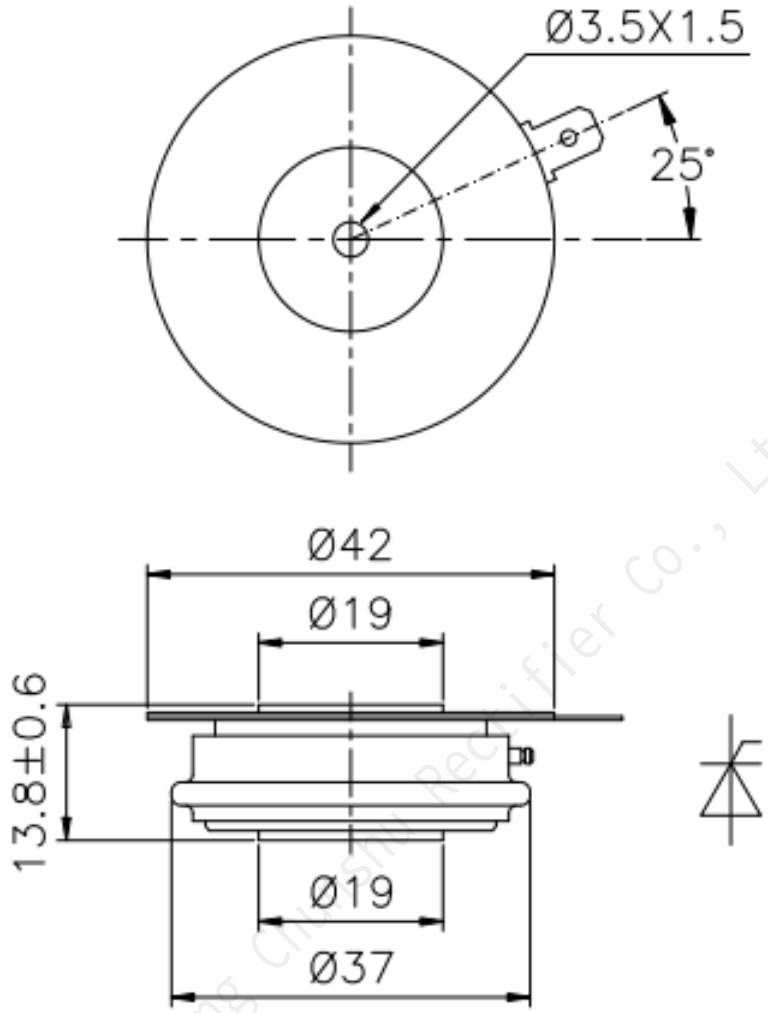
BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	1000 – 1800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	1100 – 1900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open
TRIGGERING				
I_{FGM}	Peak forward gate current	A	6	T_j=$T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	3	T_j=$T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	320	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; I_{TM}=2 I_{TAV}; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60 – 125	
T_j	Operating junction temperature	°C	-60 – 125	
MECHANICAL				
F	Mounting force	kN	9.0 – 11.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.20	T_j=25 °C; I_{TM}=1256 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.870		
I_L	Latching current, max	mA	700	T_j=25 °C; V_D=12 V; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	70	T_j=$T_{j\,max}$; V_D=V_{DRM}; V_R=V_{RRM}	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	1000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	2.50 2.00	T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 200	T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		

SWITCHING					
t_{gd}	Delay time	μs	2.00	T_j=25 °C; V_D=0.4·V_{DRM}; I_{TM}=I_{TAV}; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
t_q	Turn-off time[2)], max	μs	125	dv_D/dt=50 V/μs; T_j=$T_{j\,max}$; I_{TM}= I_{TAV}; di_R/dt=-10 A/μs; V_R=100V; V_D=0.67·V_{DRM}	
Q_{rr}	Total recovered charge, max	μC	800	T_j=$T_{j\,max}$; I_{TM}= 400 A; di_R/dt=-10 A/μs; V_R=100 V;	
t_{rr}	Reverse recovery time, typ	μs	16.0		
I_{rrM}	Peak reverse recovery current, max	A	100		
THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.040	Direct current	Double side cooled
R_{thjc-A}			0.088		Anode side cooled
R_{thjc-K}			0.072		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.008	Direct current	
MECHANICAL					
w	Weight, typ	g	110		
D_s	Surface creepage distance	mm (inch)	10.30 (0.405)		
D_a	Air strike distance	mm (inch)	6.30 (0.248)		

OVERALL DIMENSIONS



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All dimensions in millimeters

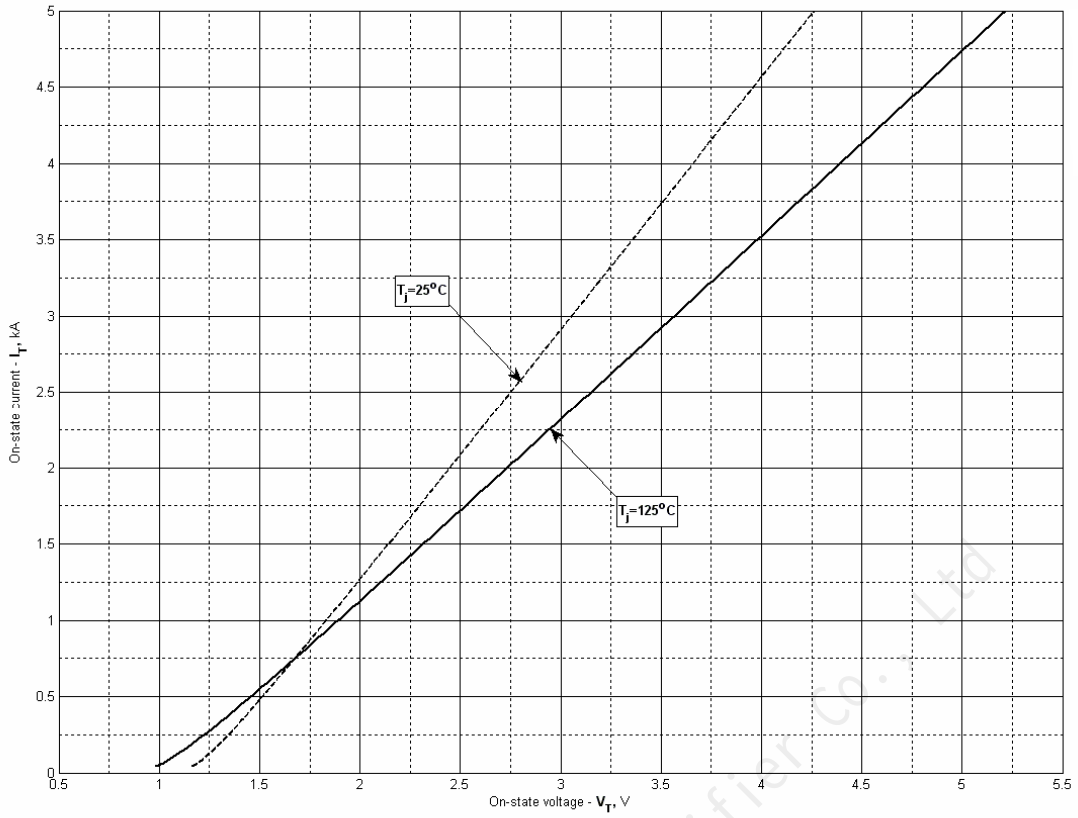

Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	1.093096	0.884269
B	0.563150	0.772462
C	-0.175856	-0.234867
D	0.298028	0.398037

On-state characteristic model (see Fig. 1)

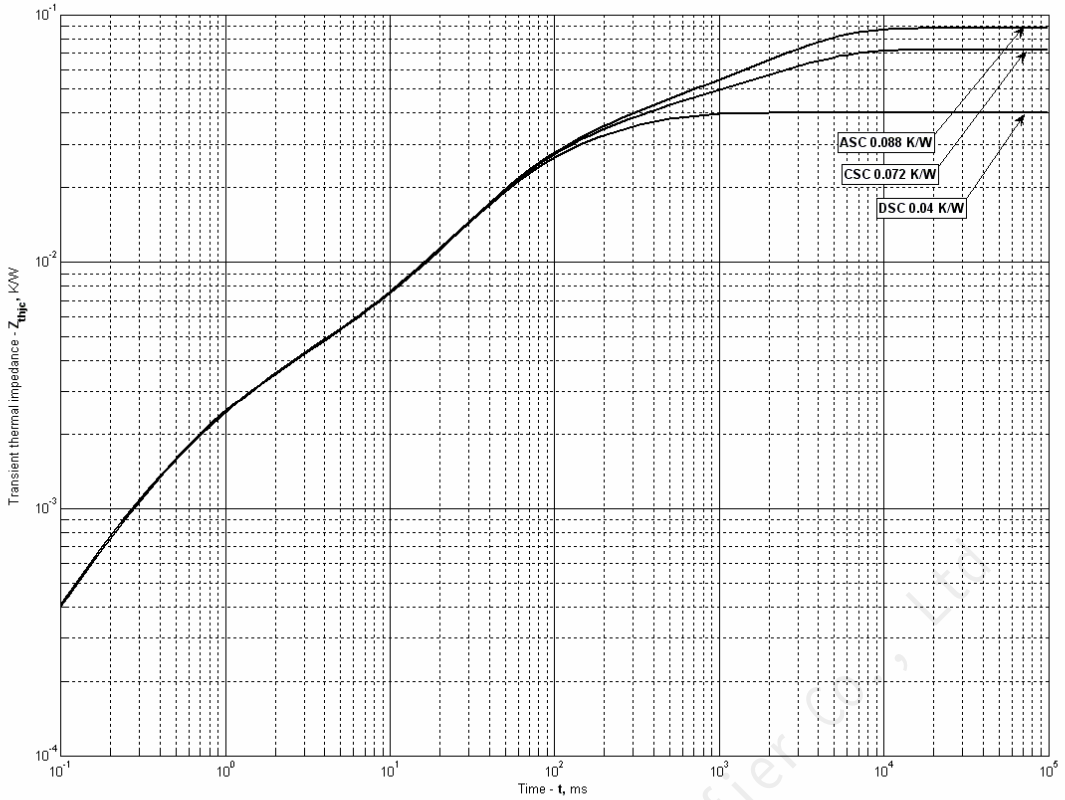

Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

$\boldsymbol{\tau_i}$ = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.01423	0.01906	0.003576	0.002535	-4.666e-005	0.0006479
$\boldsymbol{\tau_i}$, **s**	0.265	0.05901	0.03499	0.001252	0.000001	0.0002488

DC Anode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.04804	0.001789	0.01342	0.02147	0.001374	0.001945
$\boldsymbol{\tau_i}$, **s**	2.651	0.4195	0.2622	0.05451	0.002585	0.0005847

DC Cathode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.03216	0.01306	0.002934	0.02064	0.001493	0.001786
$\boldsymbol{\tau_i}$, **s**	2.647	0.2831	0.1455	0.05284	0.002255	0.0005519

Transient thermal impedance junction to case $\mathbf{Z_{thjc}}$ model (see Fig. 2)

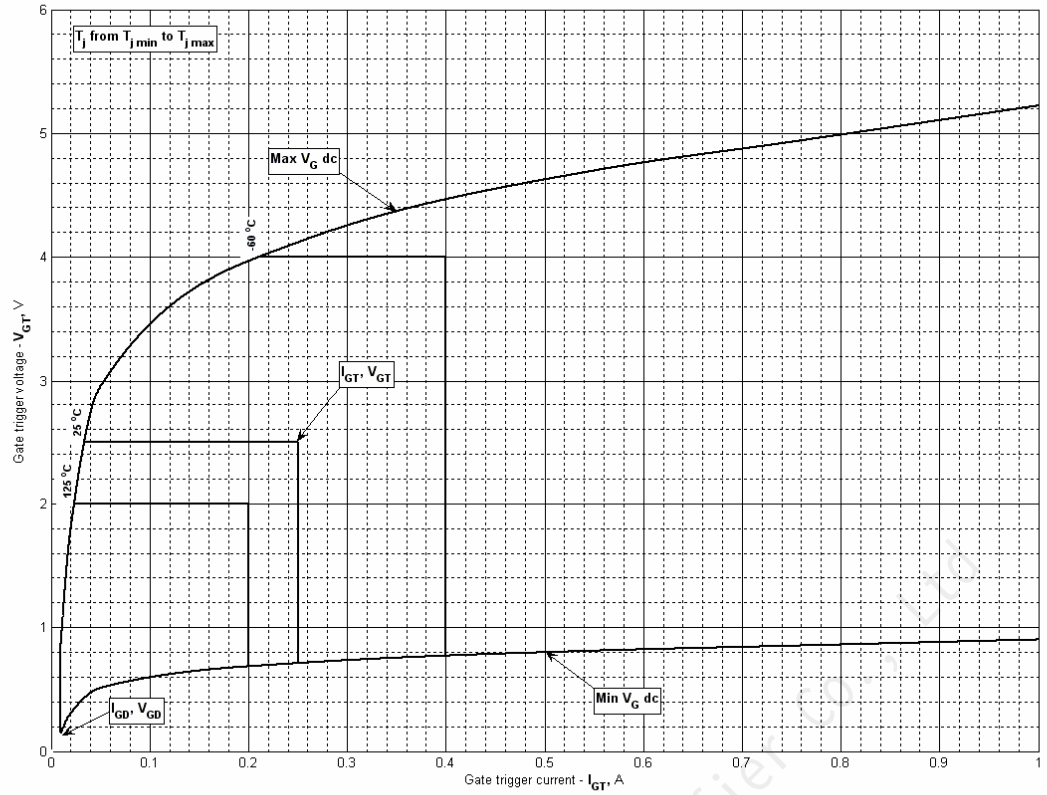

Fig 3 – Gate characteristics – Trigger limits

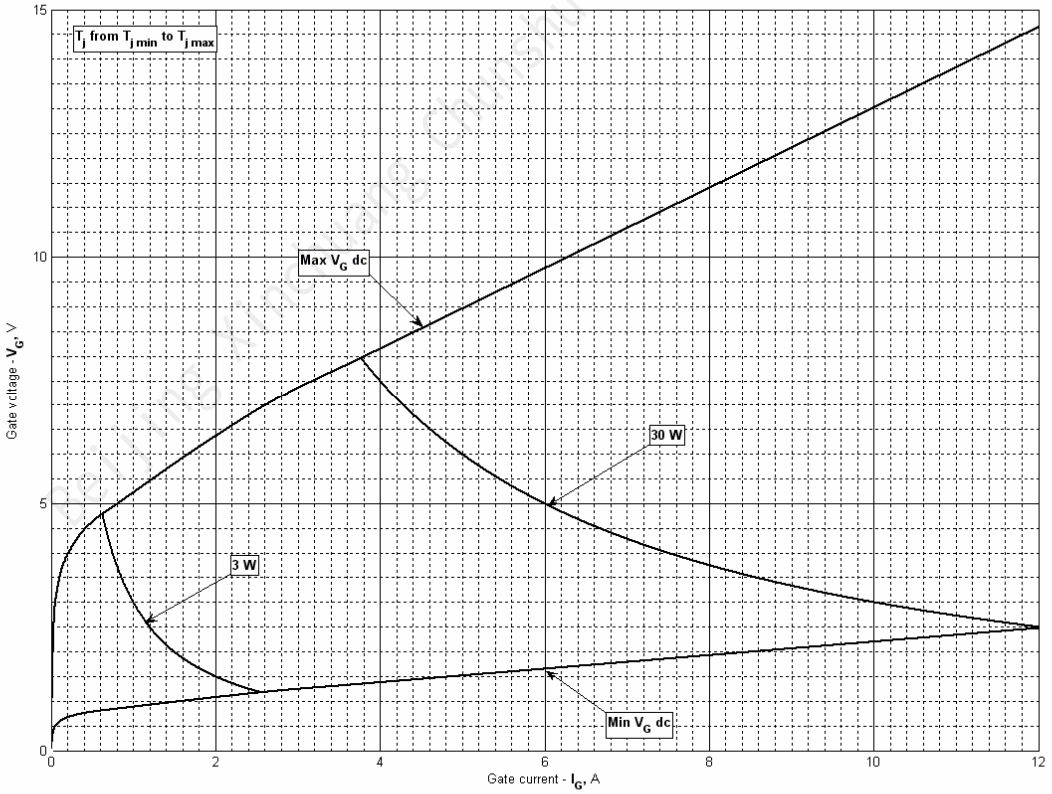

Fig 4 - Gate characteristics –Power curves

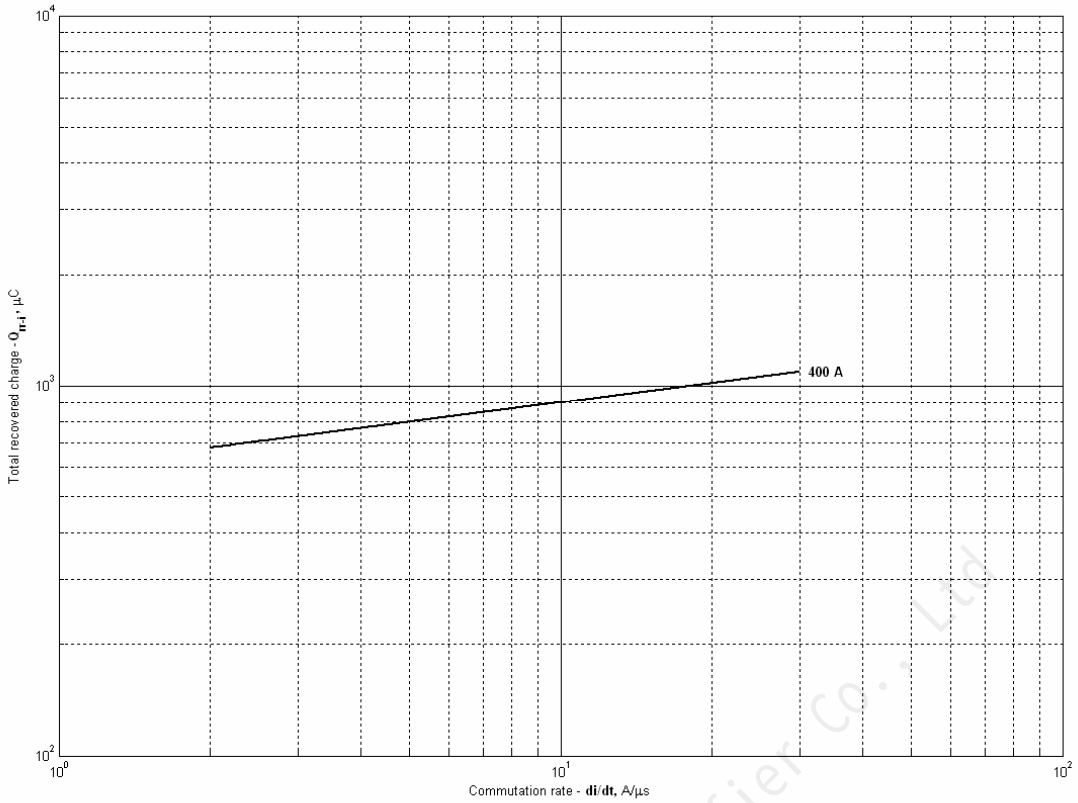

Fig 5 – Total recovered charge, Q_{rr-i} (integral)

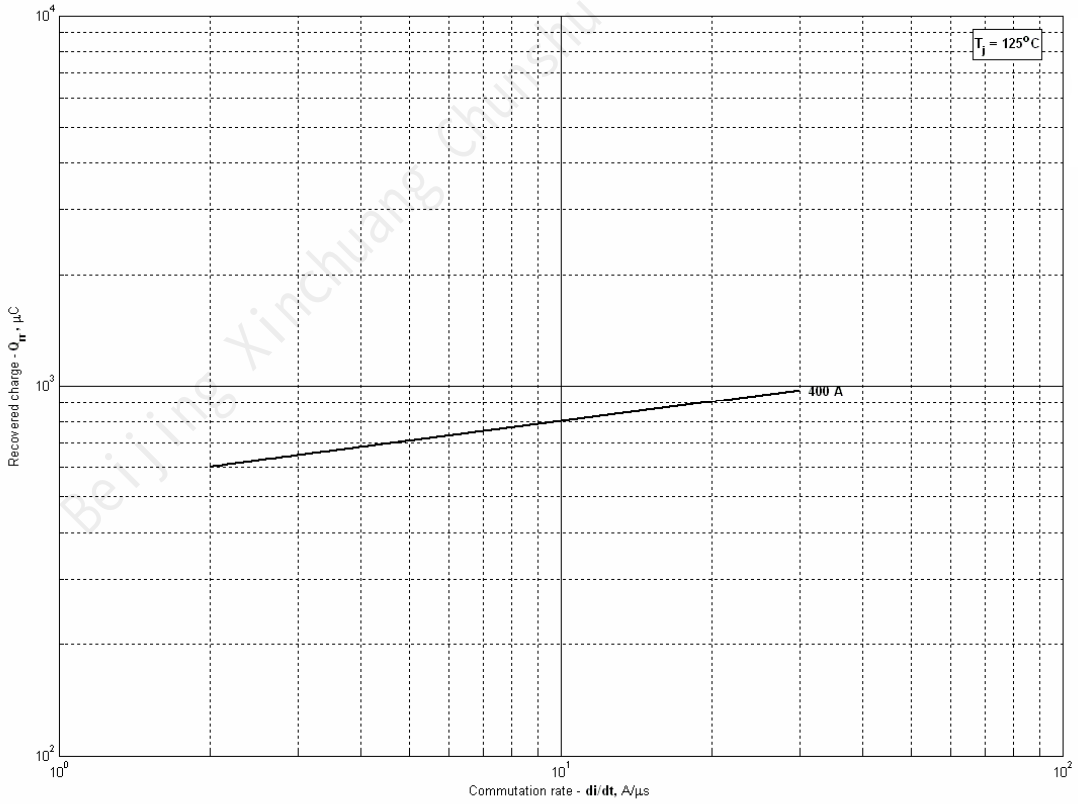

Fig 6 - Recovered charge, Q_{rr} (linear)

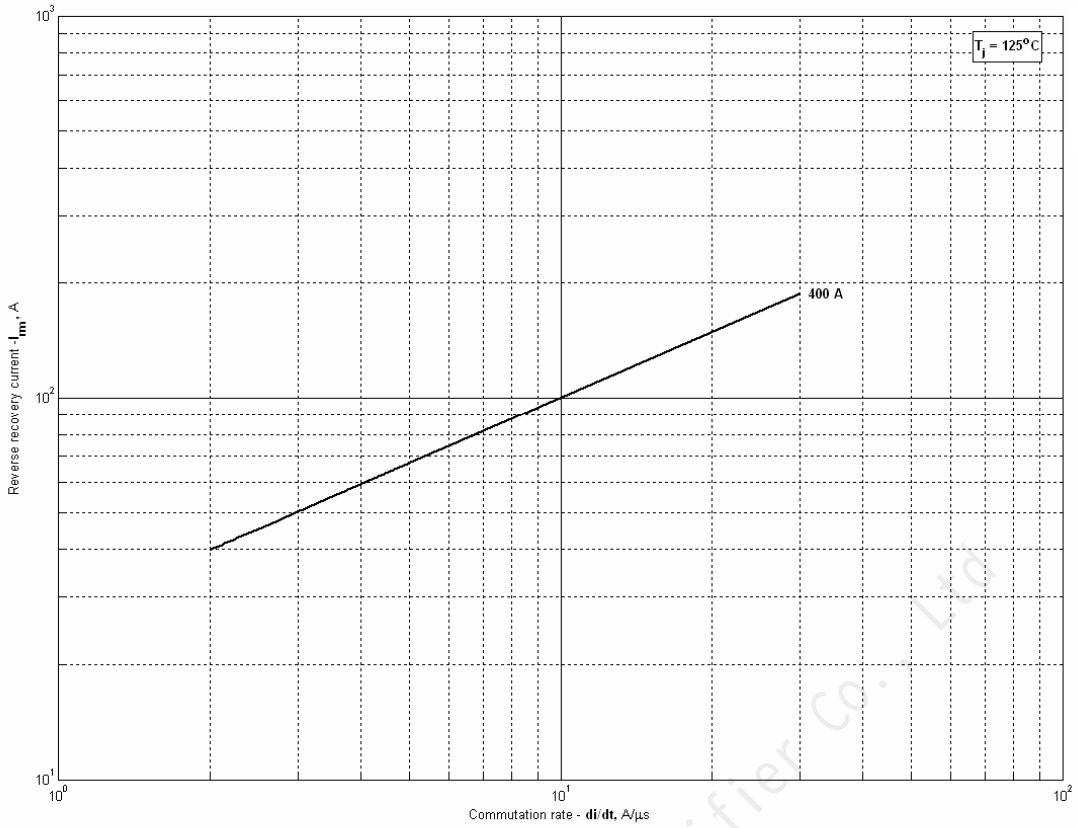

Fig 7 – Peak reverse recovery current, I_{rm}

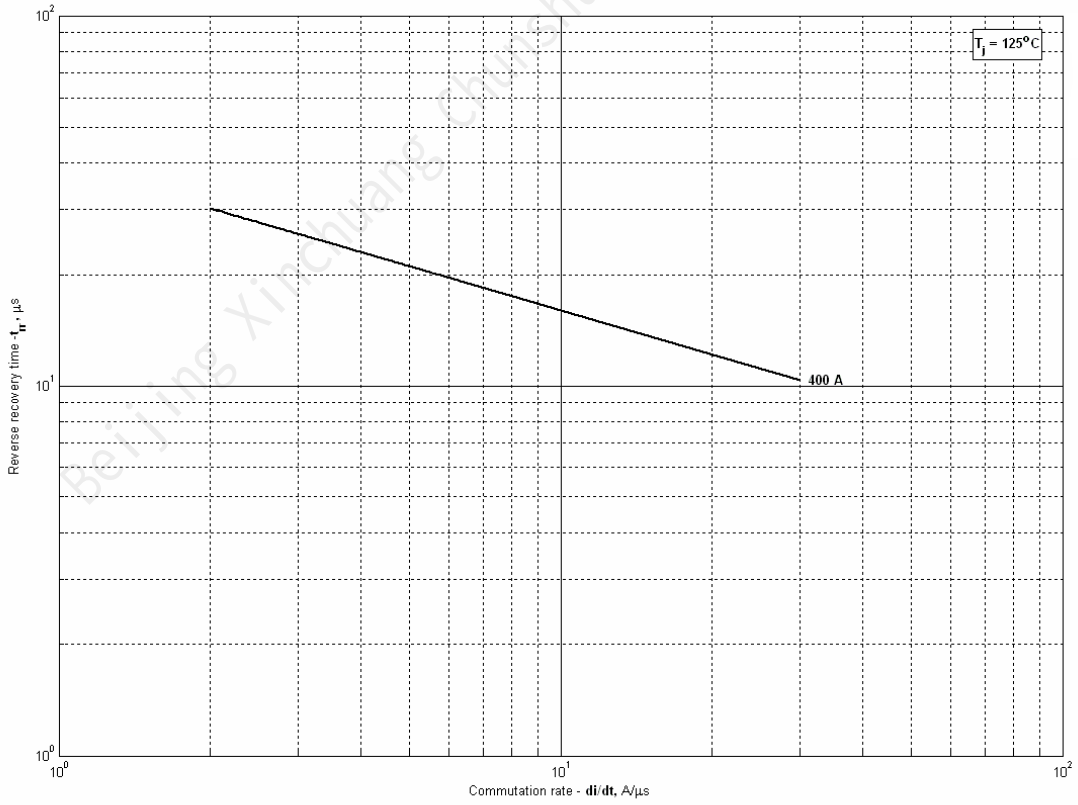

Fig 8 – Maximum recovery time, t_{rr} (linear)

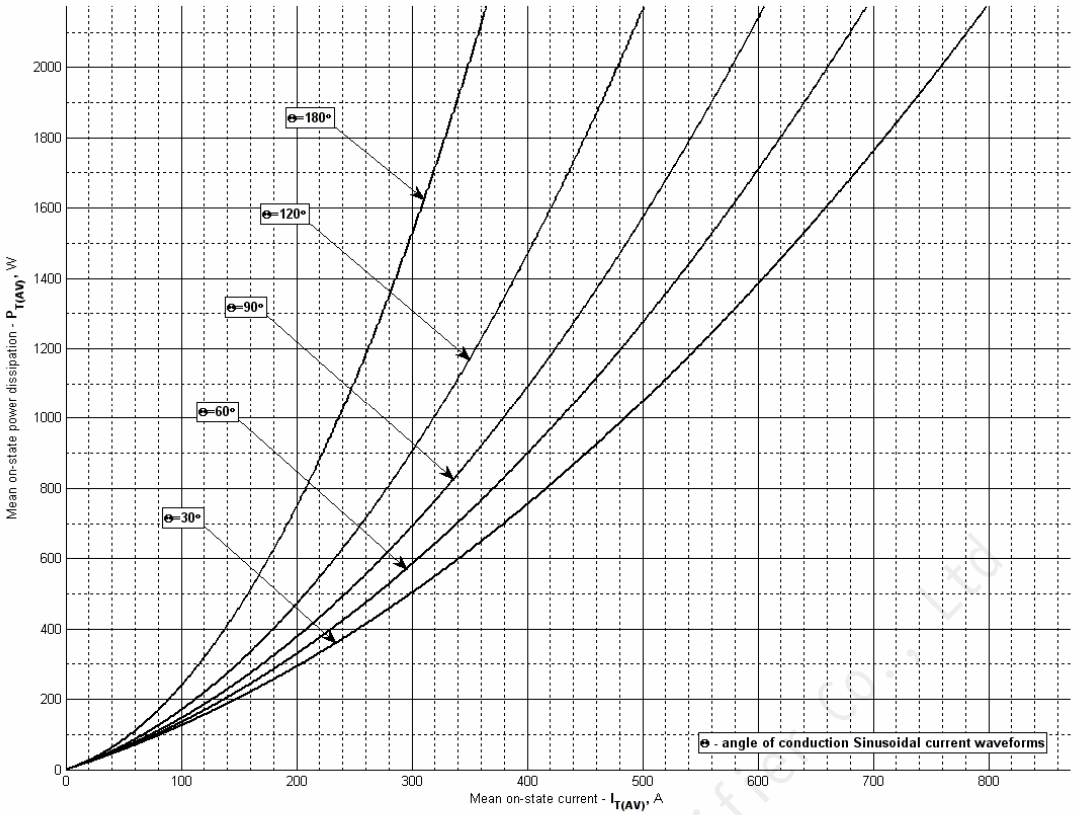

Fig 9 – On-state power loss (sinusoidal current waveforms)

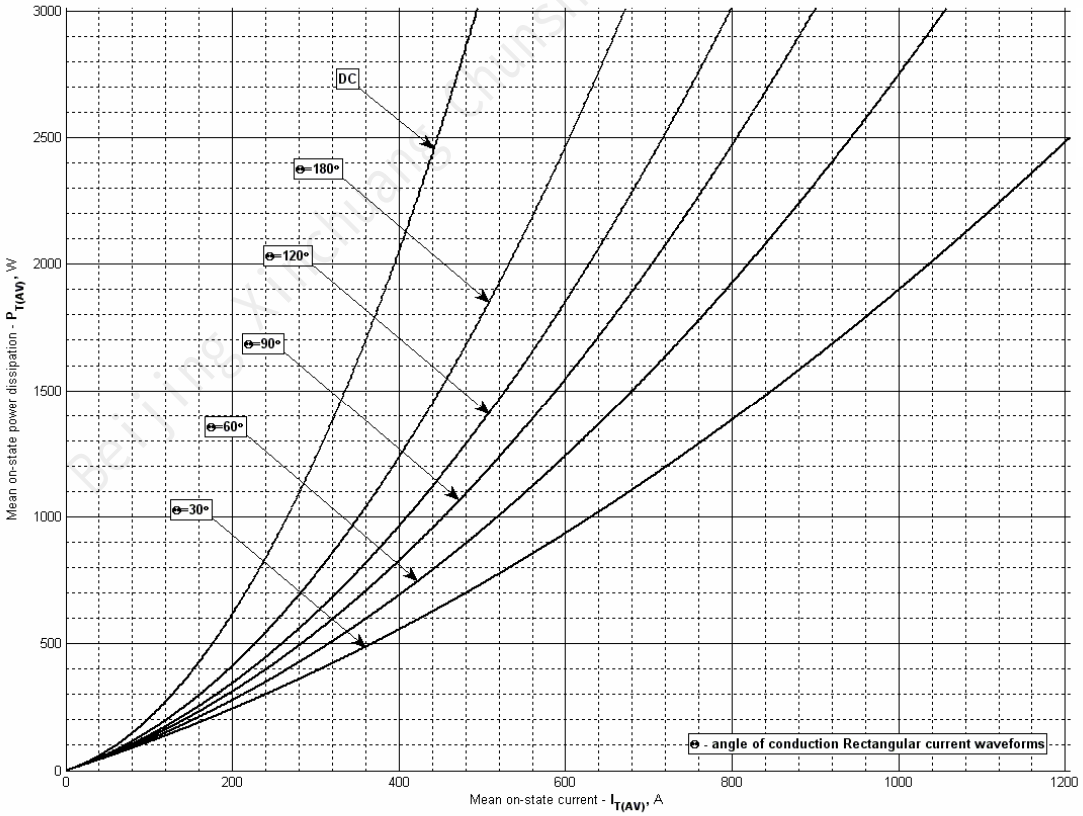

Fig 10 – On-state power loss (rectangular current waveforms)

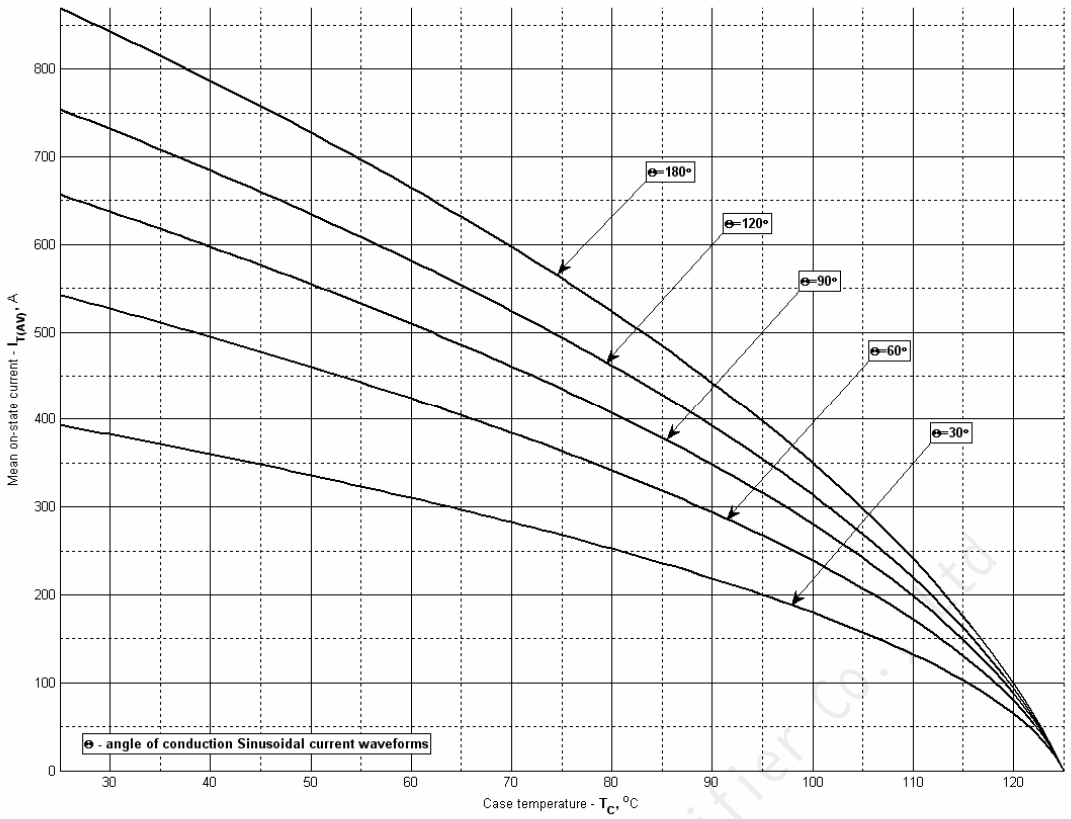

Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

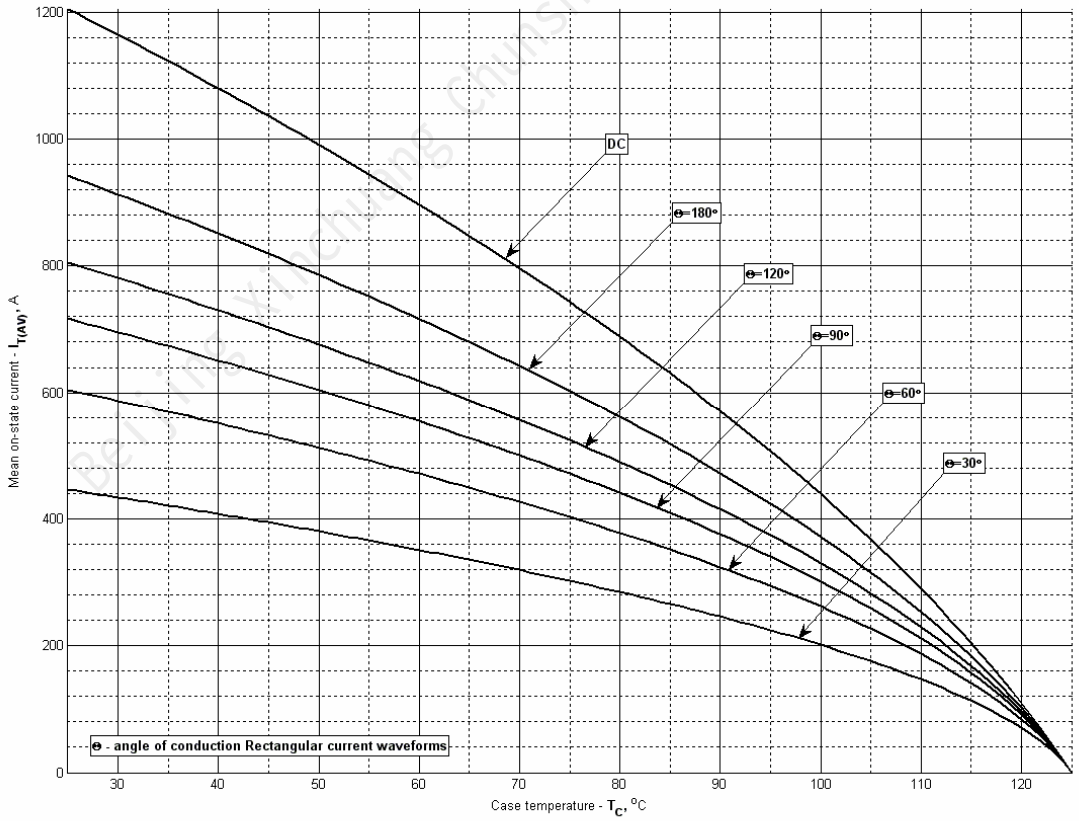

Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

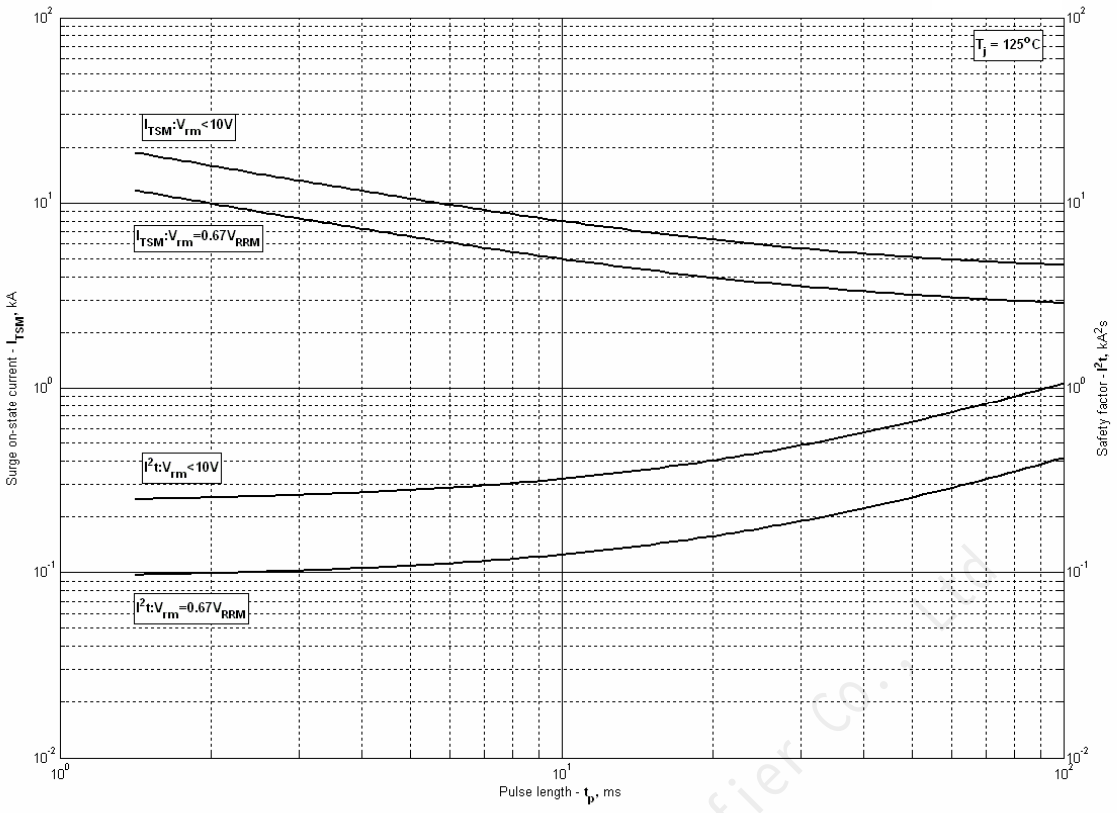

Fig 13 – Maximum surge and I t ratings

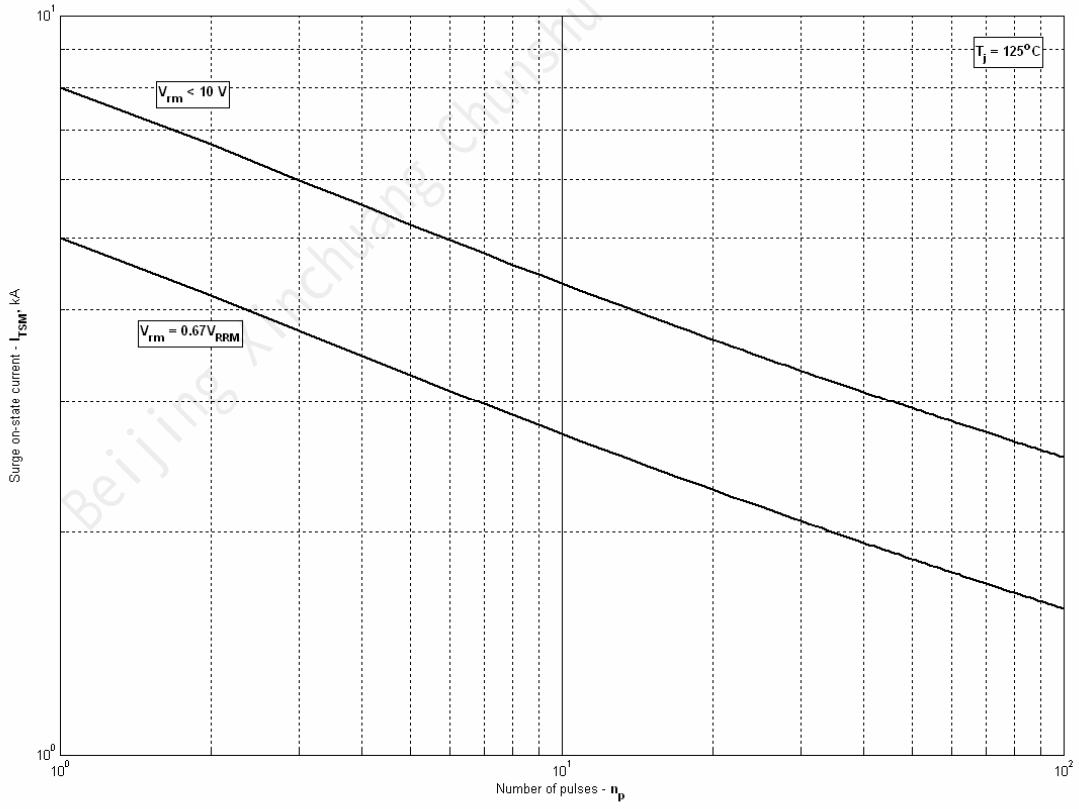

Fig 14 – Maximum surge ratings

