ChunZheng

High-end Power Semiconductor Manufacturer

KP500A 2000V-2800V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current			I_{TAV}	500 A	
Repetitive peak off-state voltage			V_{DRM}	2000 – 2800 V	
Repetitive peak reverse voltage			V_{RRM}		
Turn-off time			t_q	250 μs	
V_{DRM}, V_{RRM}, V	2000	2200	2400	2600	2800
Voltage code	20	22	24	26	28
T_j, °C	-60 – 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	500	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	785	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	10.0 12.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			11.0 13.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
I^2t	Safety factor	A^2s	0.247×10^6	T_j=$T_{j\,max}$	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_R=0.67·V_{RRM}; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			0.500×10^6 0.720×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
			0.500×10^6 0.700×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs

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BLOCKING				
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000–2800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100–2900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open
TRIGGERING				
I_{FGM}	Peak forward gate current	A	8	T_j=$T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	T_j=$T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	400	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; I_{TM}=2 I_{TAV}; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60–125	
T_j	Operating junction temperature	°C	-60–125	
MECHANICAL				
F	Mounting force	kN	14.0–16.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.20	T_j=25 °C; I_{TM}=1570 A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.09	T_j=$T_{j\,max}$; 0.5 π I_{TAV} < I_T < 1.5 π I_{TAV}	
r_T	On-state slope resistance, max	mΩ	0.755		
I_L	Latching current, max	mA	1000	T_j=25 °C; V_D=12 V; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
I_H	Holding current, max	mA	300	T_j=25 °C; V_D=12 V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	100	T_j=$T_{j\,max}$; V_D=V_{DRM}; V_R=V_{RRM}	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	1000	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	2.50 2.00	T_j=25 °C T_j= $T_{j\,max}$	V_D=12 V; I_D=3 A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 200	T_j= 25 °C T_j= $T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	T_j=$T_{j\,max}$; V_D=0.67·V_{DRM}; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		

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SWITCHING					
t_{gd}	Delay time	μs	2.50	T_j=25 °C; V_D=0.4·V_{DRM}; I_{TM}=I_{TAV}; Gate pulse: I_G=I_{FGM}; V_G=20 V; t_{GP}=500 μs; di_G/dt=1 A/μs	
t_q	Turn-off time[2)], max	μs	250	dv_D/dt=50 V/μs; T_j=$T_{j\,max}$; I_{TM}= I_{TAV}; di_R/dt=-10 A/μs; V_R=100V; V_D=0.67·V_{DRM}	
Q_{rr}	Total recovered charge, max	μC	1950	T_j=$T_{j\,max}$; I_{TM}= 500 A; di_R/dt=-10 A/μs; V_R=100 V;	
t_{rr}	Reverse recovery time, typ	μs	26.0		
I_{rrM}	Peak reverse recovery current, max	A	150		
THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0320	Direct current	Double side cooled
R_{thjc-A}			0.0704		Anode side cooled
R_{thjc-K}			0.0576		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0060	Direct current	
MECHANICAL					
w	Weight, typ	g	260		
D_s	Surface creepage distance	mm (inch)	19.44 (0.765)		
D_a	Air strike distance	mm (inch)	12.10 (0.476)		

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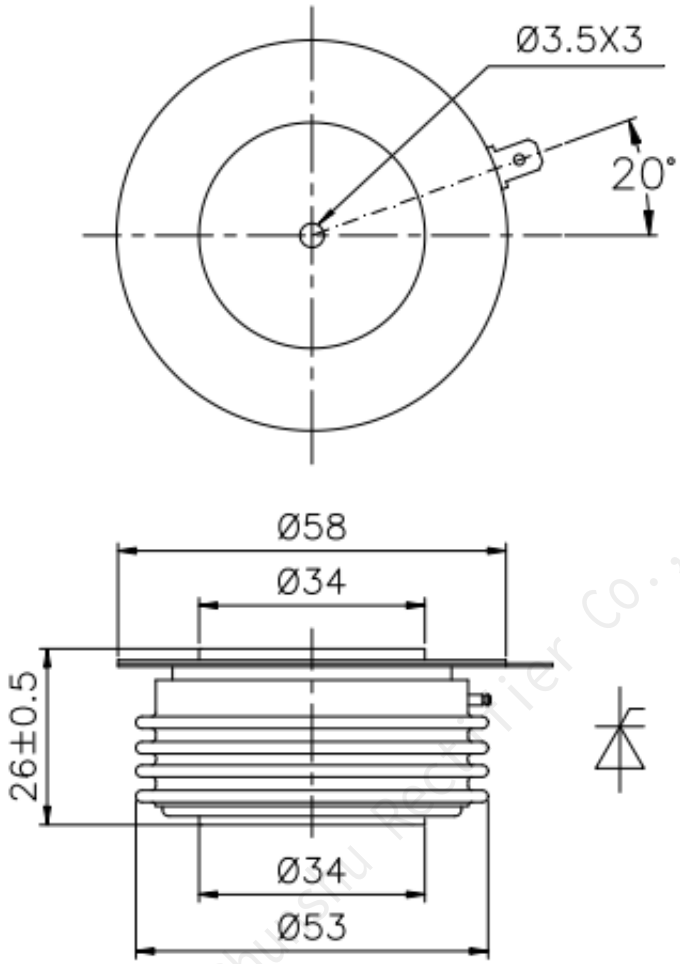
OVERALL DIMENSIONS



KT40

All dimensions in millimeters

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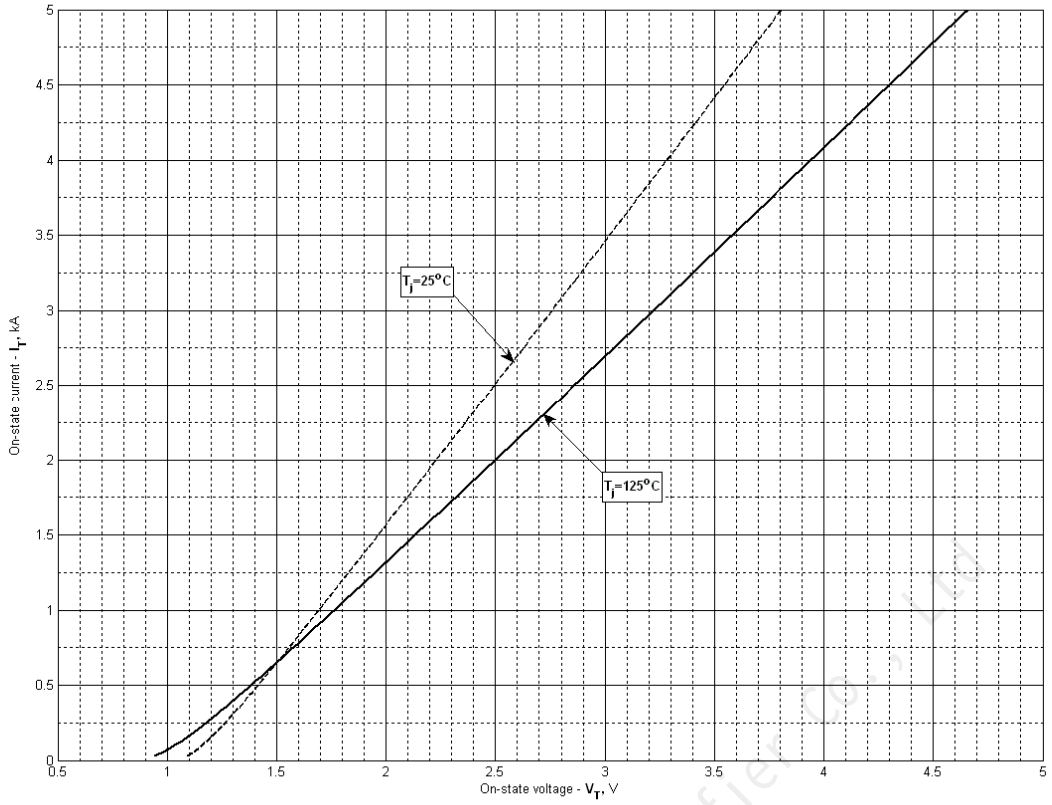

Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	1.031292	0.861860
B	0.483787	0.663978
C	-0.181345	-0.242199
D	0.304070	0.406107

On-state characteristic model (see Fig. 1)

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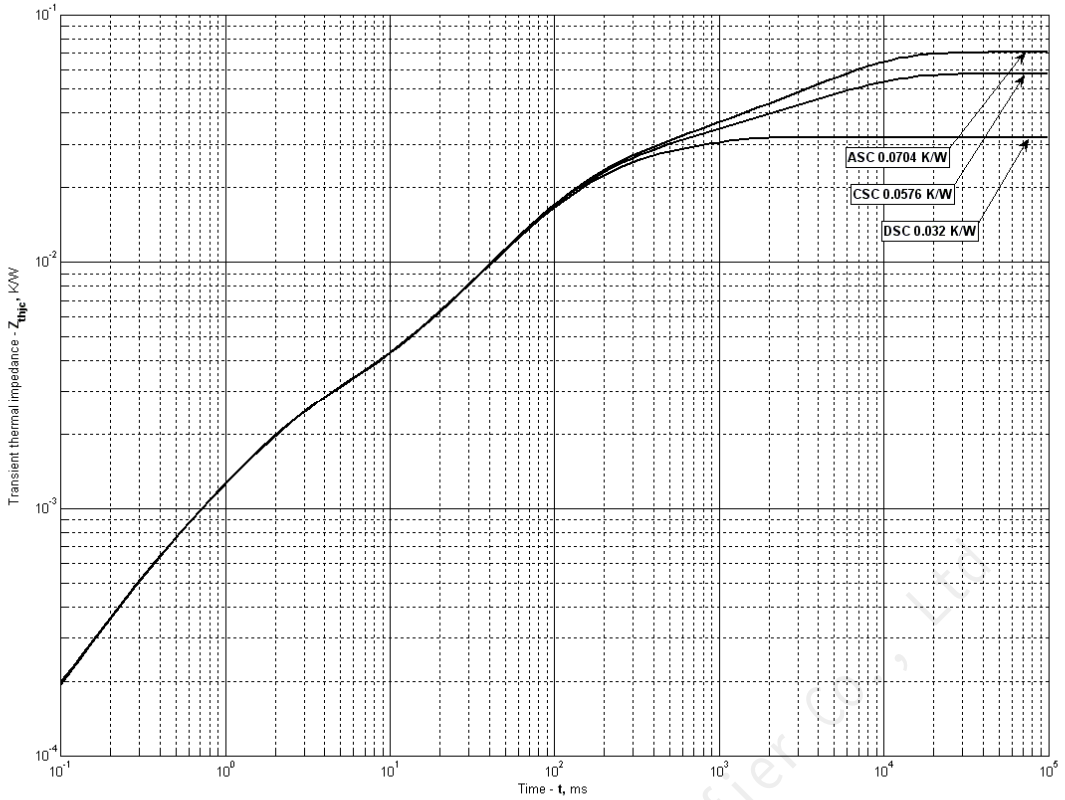

Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

Z_{thjc} = Thermal resistance at time t.

R_i = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i, K/W	0.000005619	0.01031	0.01922	0.0004148	0.001895	0.0001521
τ_i, s	7.790	0.5094	0.09719	0.01725	0.0016	0.0002257

DC Anode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.0381	0.008681	0.01867	0.001961	0.0001787	0.002771
τ_i, s	5.351	0.4584	0.09325	0.001734	0.0002174	0.9059

DC Cathode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.02561	0.001472	0.01786	0.001926	0.0001928	0.01052
τ_i, s	5.328	0.1832	0.09031	0.001714	0.0002598	0.525

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

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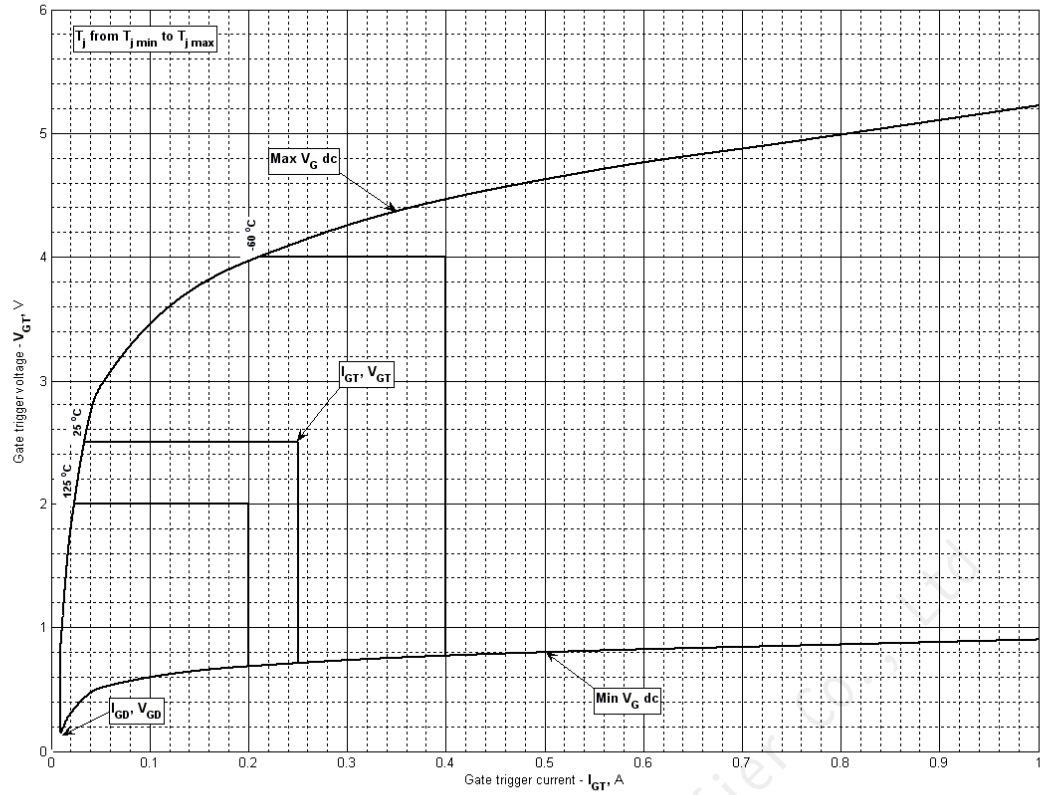

Fig 3 – Gate characteristics – Trigger limits

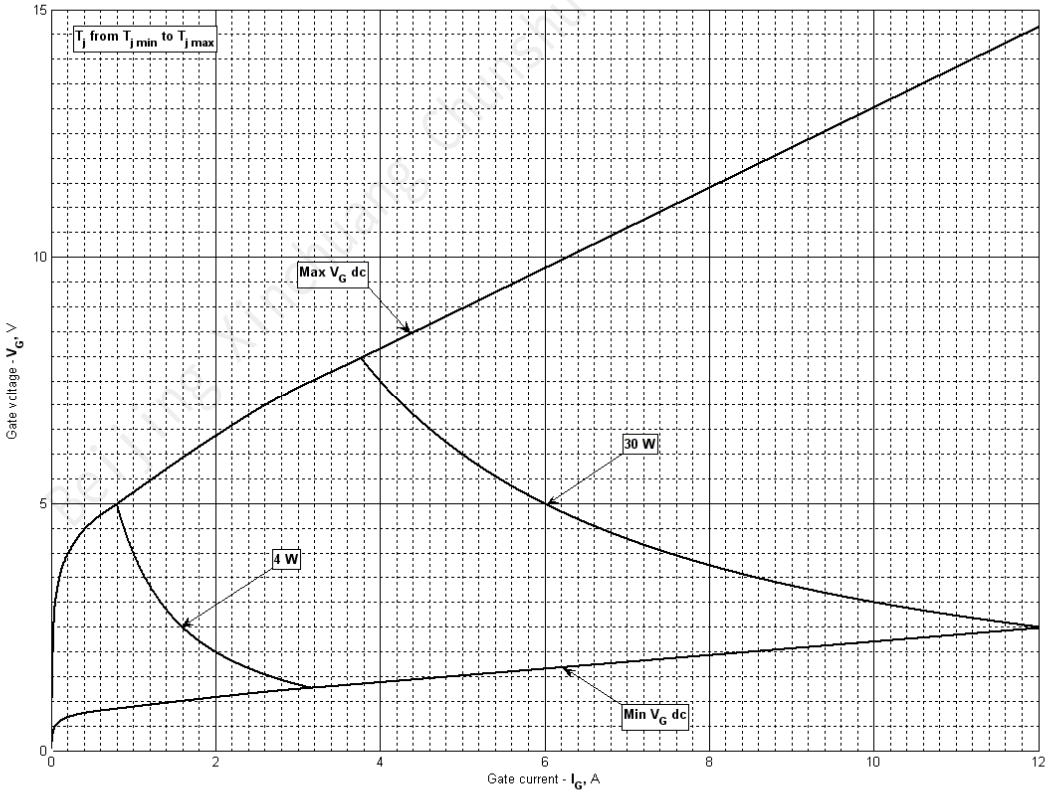

Fig 4 - Gate characteristics –Power curves

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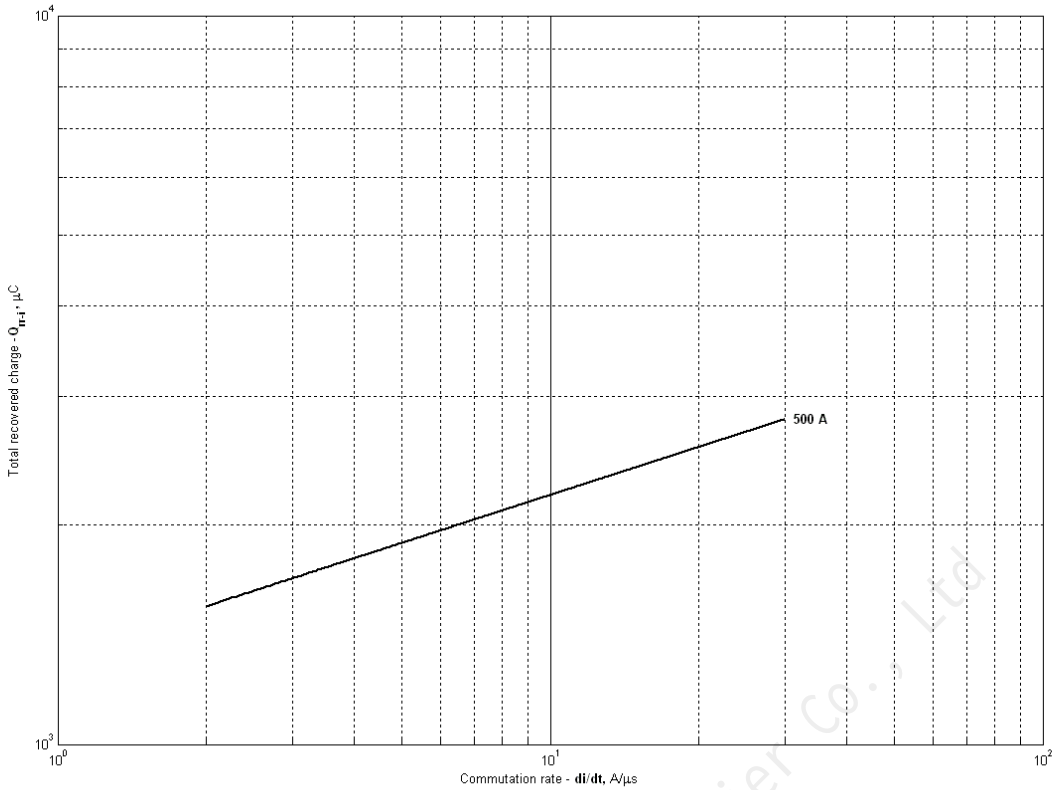

Fig 5 – Total recovered charge, Q_{rr-i} (integral)

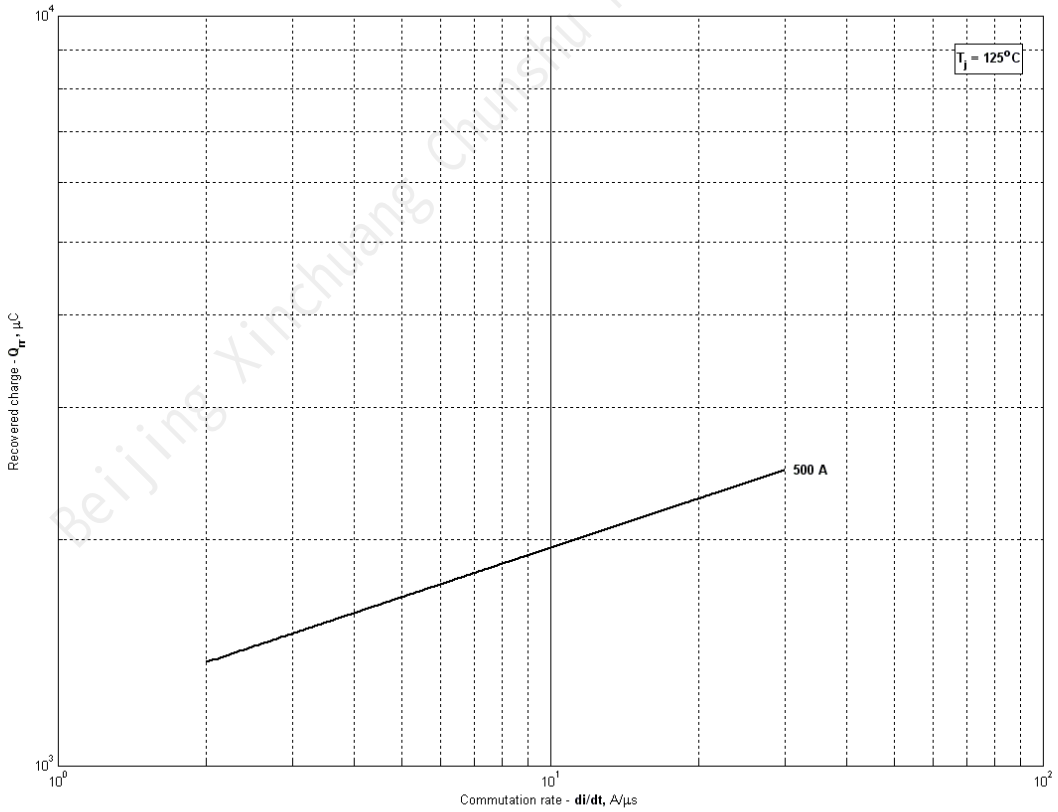

Fig 6 - Recovered charge, Q_{rr} (linear)

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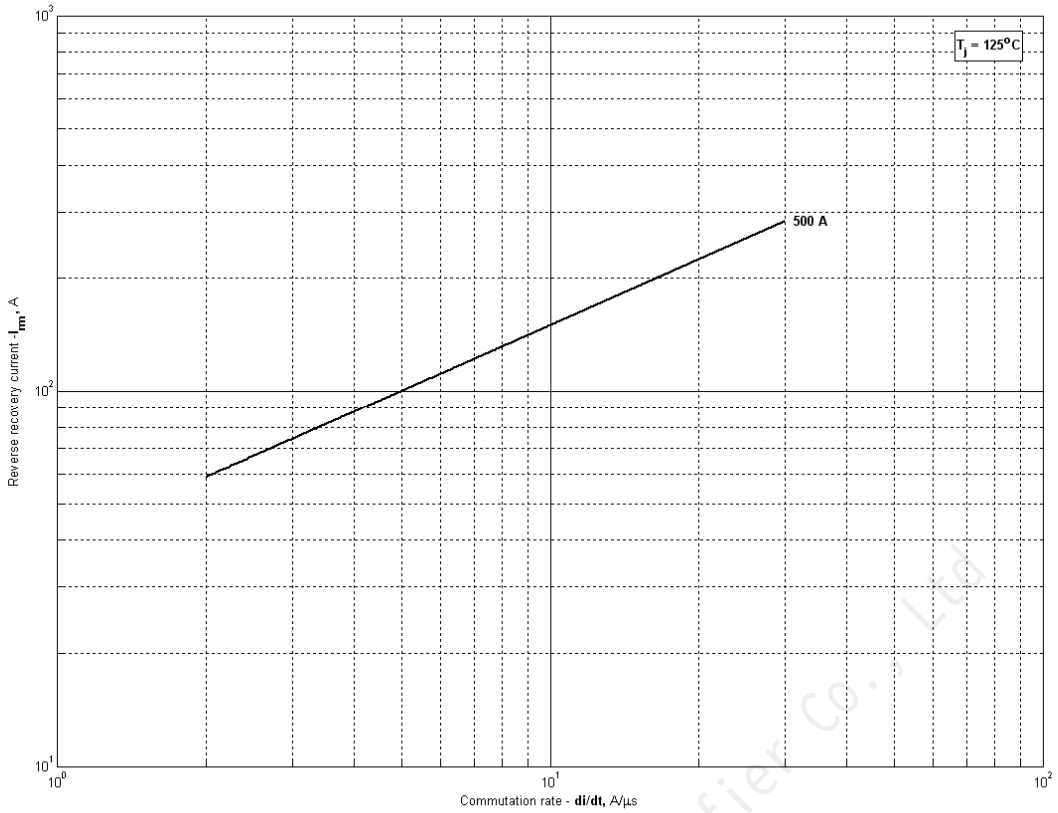

Fig 7 – Peak reverse recovery current, I

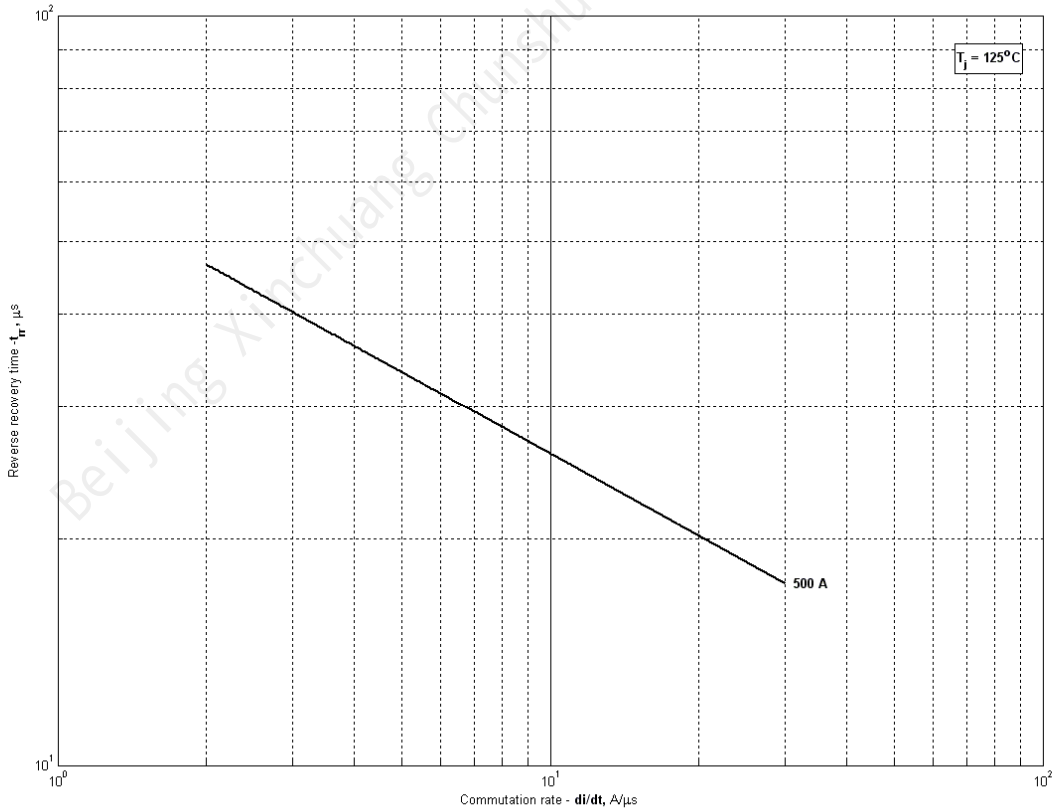

Fig 8 – Maximum recovery time, t_{rr} (linear)

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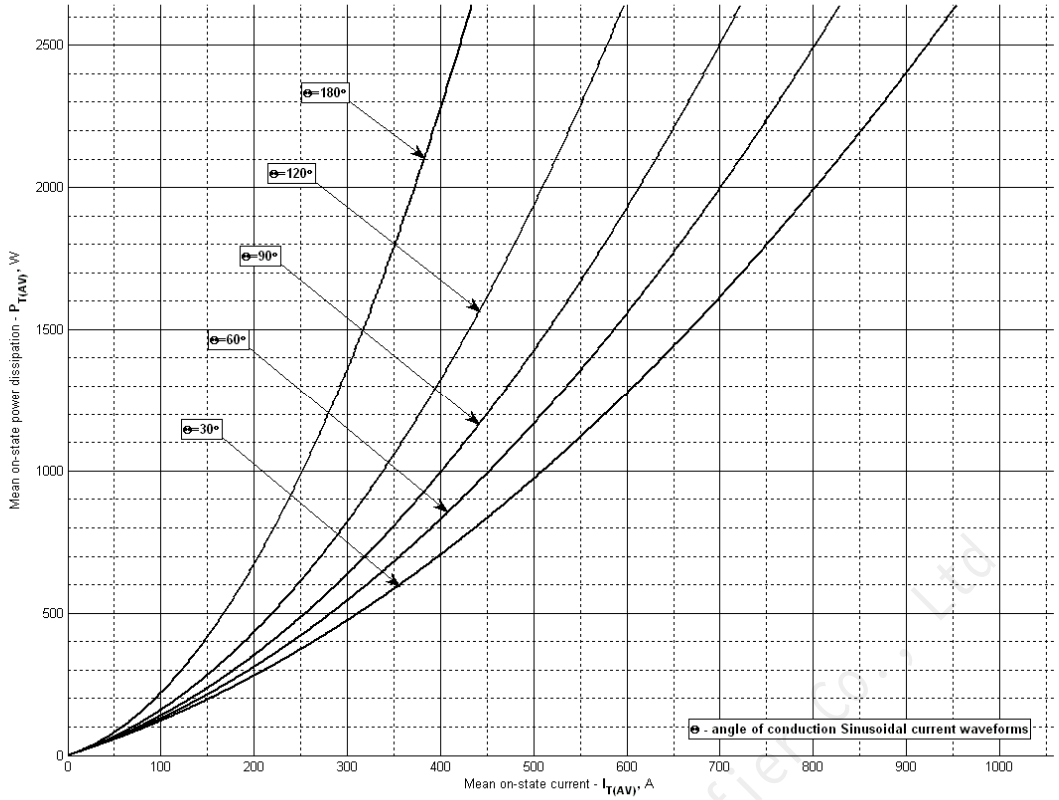

Fig 9 – On-state power loss (sinusoidal current waveforms)

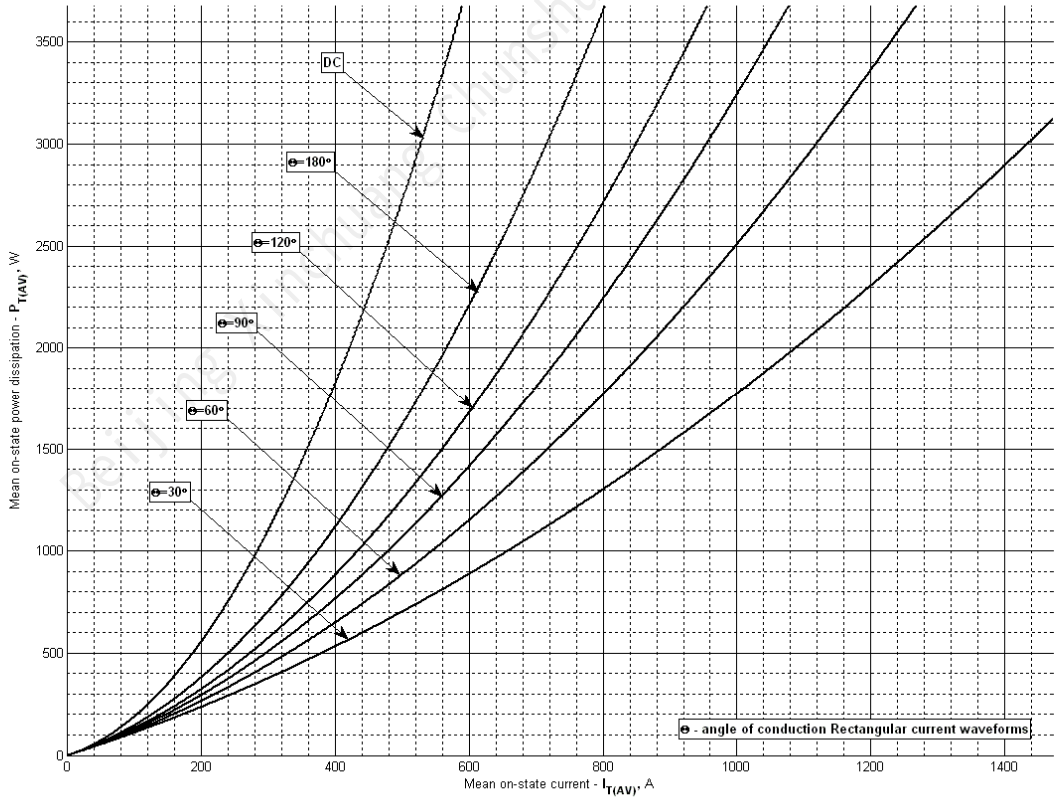

Fig 10 – On-state power loss (rectangular current waveforms)

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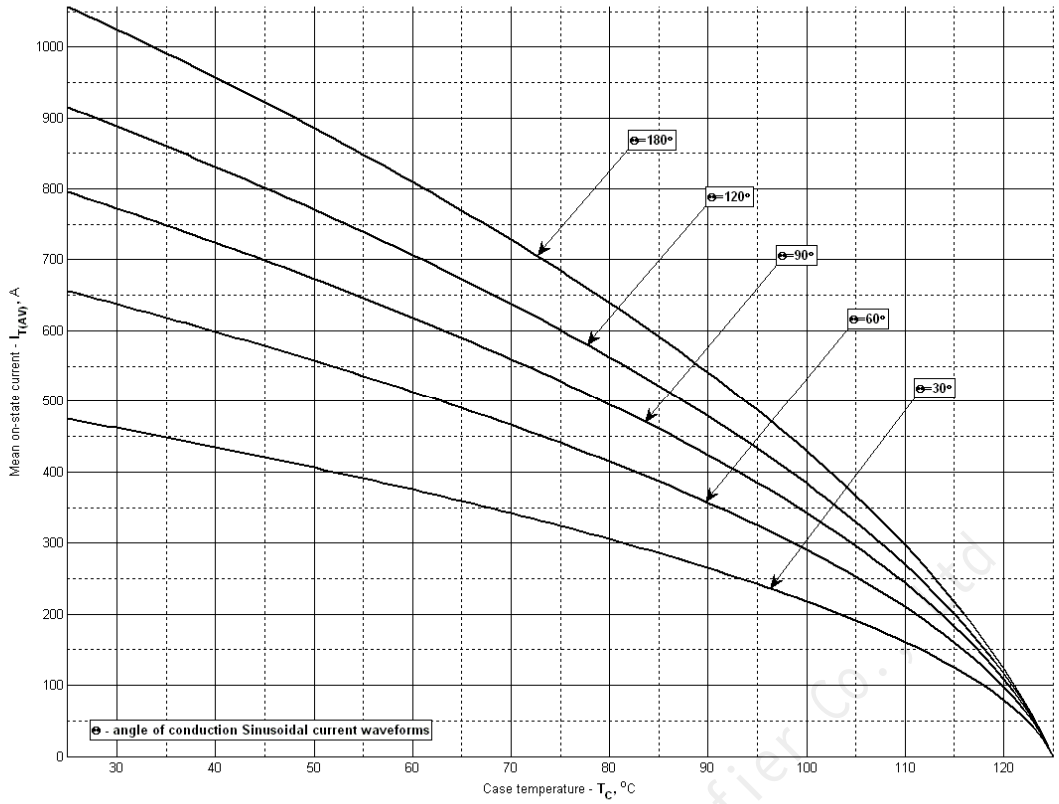

Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

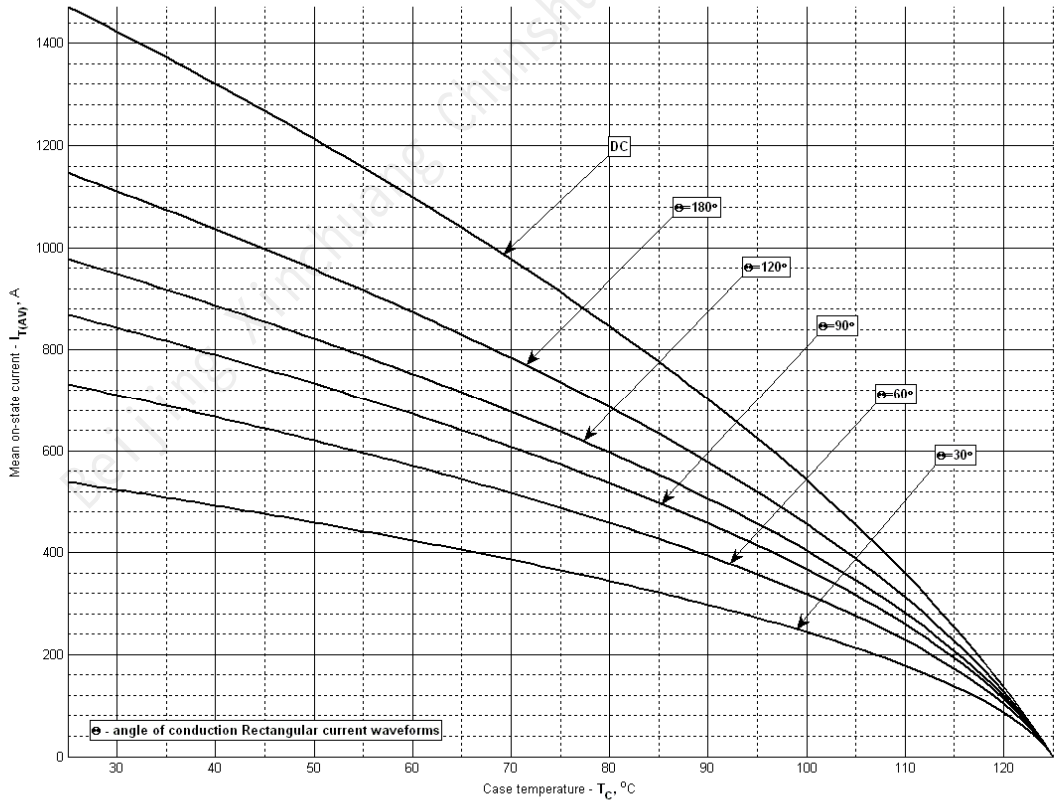

Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

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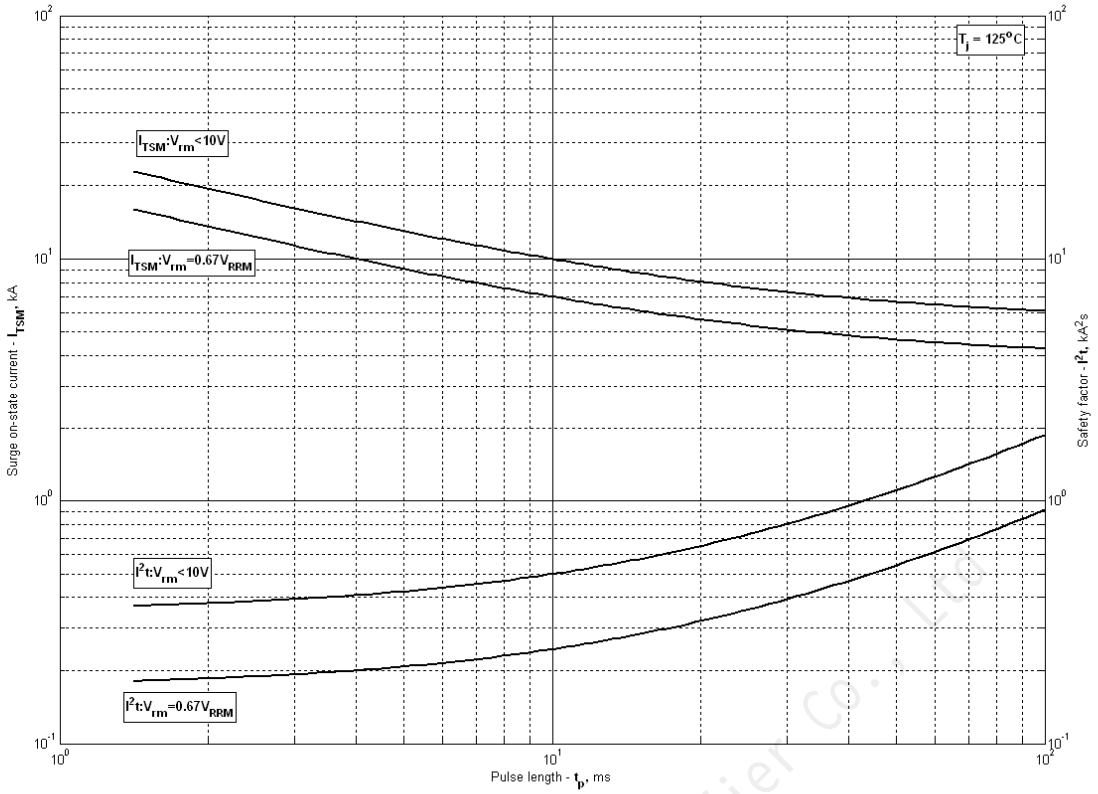

Fig 13 – Maximum surge and I

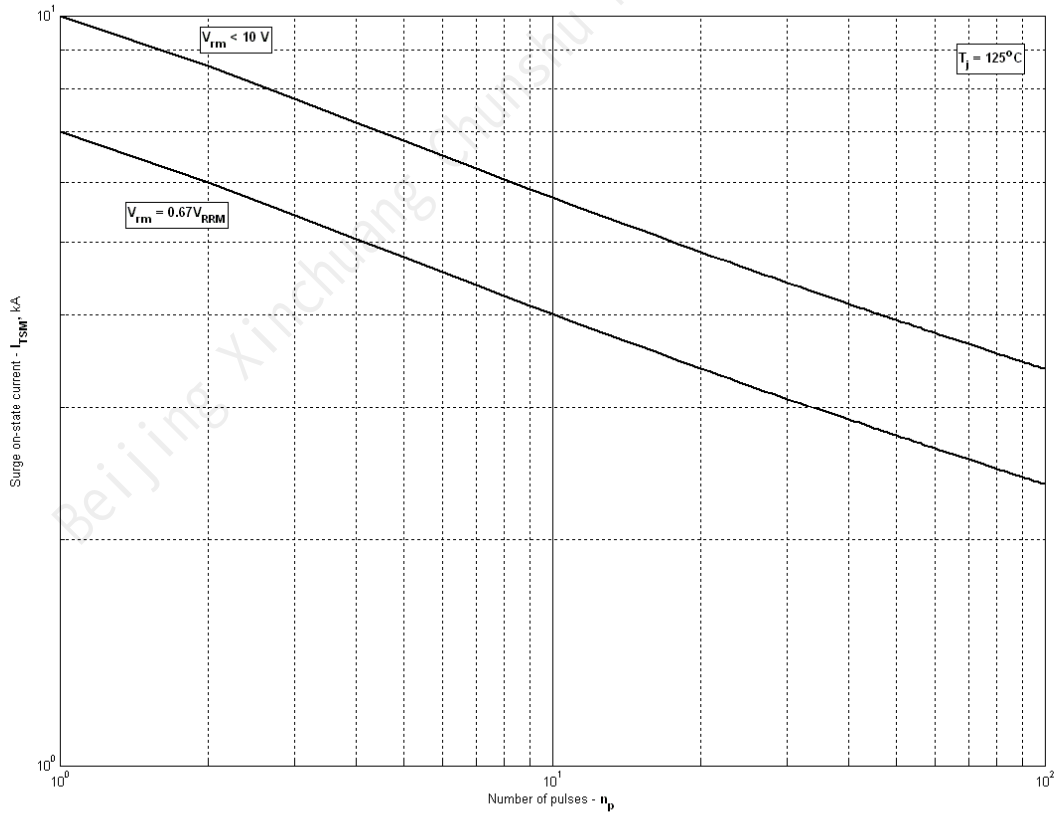

Fig 14 – Maximum surge ratings

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