ChunZheng

High-end Power Semiconductor Manufacturer

KP800A 3500V-4400V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current		I_{TAV}	800 A	
Repetitive peak off-state voltage		V_{DRM}	3500 – 4400 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	500 µs	
V_{DRM}, V_{RRM}, V	3500	4000	4200	4400
Voltage code	35	40	42	44
T_j, °C	-60 – 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	800	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	1256	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	15.0 17.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
			16.0 18.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
I^2t	Safety factor	A^2s	1.125×10^6 1.445×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
			1.060×10^6 1.340×10^6	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse:I_G=I_{FGM}; V_G=20 V; t_{GP}=500 µs; di_G/dt=1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	3500–4400	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	3600–4500	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

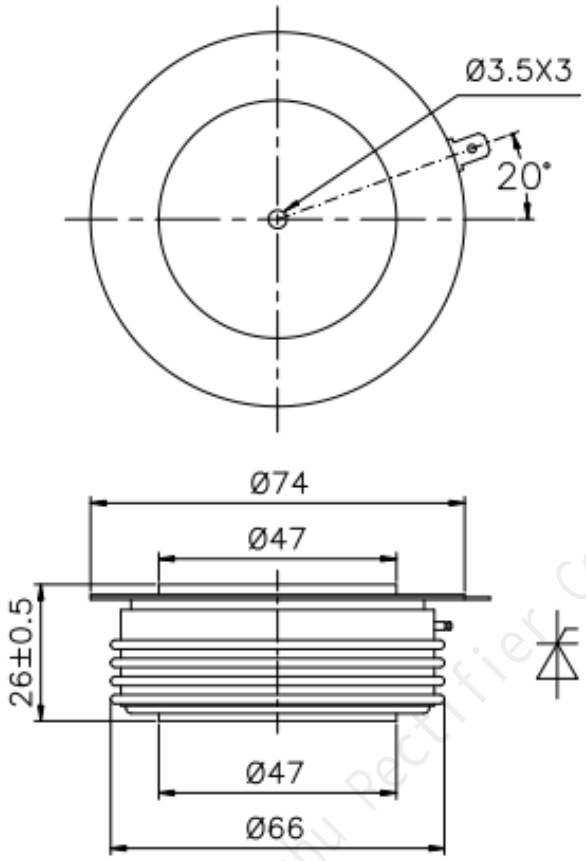
TRIGGERING				
P_{GM}	Peak forward gate power	W	40	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	4	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	630	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=500$ μs; $di_G/dt=1$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60−125	
T_j	Operating junction temperature	°C	-60−125	
MECHANICAL				
F	Mounting force	kN	24.0−28.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.80	$T_j=25$ °C; $I_{TM}=2512$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.25	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	0.670		
I_L	Latching current, max	mA	1500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=500$ μs; $di_G/dt=1$ A/μs	
I_H	Holding current, max	mA	1000	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	150	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	1000	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	2.50 2.00	$T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	250 200	$T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.25	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	10.00		
SWITCHING					
t_{gd}	Delay time	μs	3.50	$T_j=25$ °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=I_{FGM}$; $V_G=20$ V; $t_{GP}=500$ μs; $di_G/dt=1$ A/μs	
t_q	Turn-off time[2)], max	μs	500	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=800$ A; $di_R/dt=-10$ A/μs; $V_R=100$V; $V_D=0.67\cdot V_{DRM}$	
Q_{rr}	Total recovered charge, max	μC	3500	$T_j=T_{j\,max}$; $I_{TM}=800$ A; $di_R/dt=-10$ A/μs; $V_R=100$ V;	
t_{rr}	Reverse recovery time, typ	μs	40.0		
I_{rrM}	Peak reverse recovery current, max	A	175		

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0180	Direct current	Double side cooled
R_{thjc-A}			0.0396		Anode side cooled
R_{thjc-K}			0.0324		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0040	Direct current	
MECHANICAL					
w	Weight, typ	g	510		
D_s	Surface creepage distance	mm (inch)	31.60 (1.244)		
D_a	Air strike distance	mm (inch)	16.50 (0.649)		

OVERALL DIMENSIONS



KT55

All dimensions in millimeters

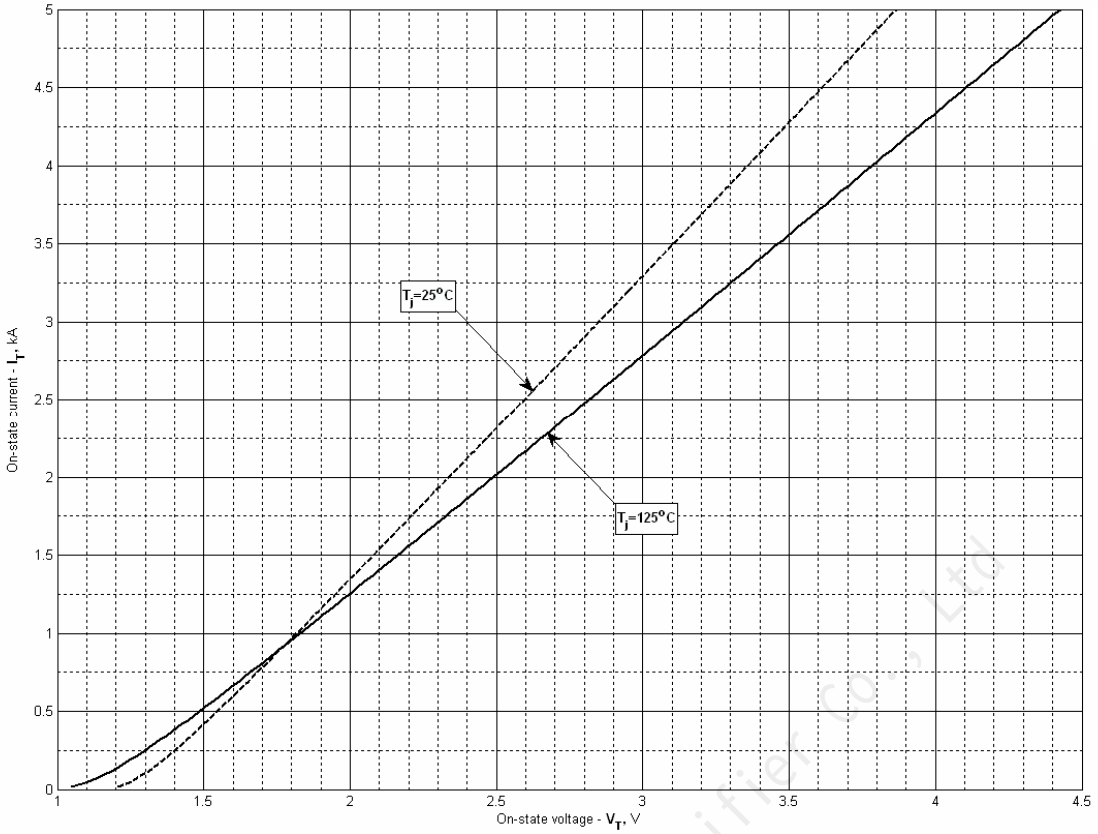


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	1.166319	0.995217
B	0.466815	0.588679
C	-0.196880	-0.262947
D	0.320994	0.428711

On-state characteristic model (see Fig. 1)

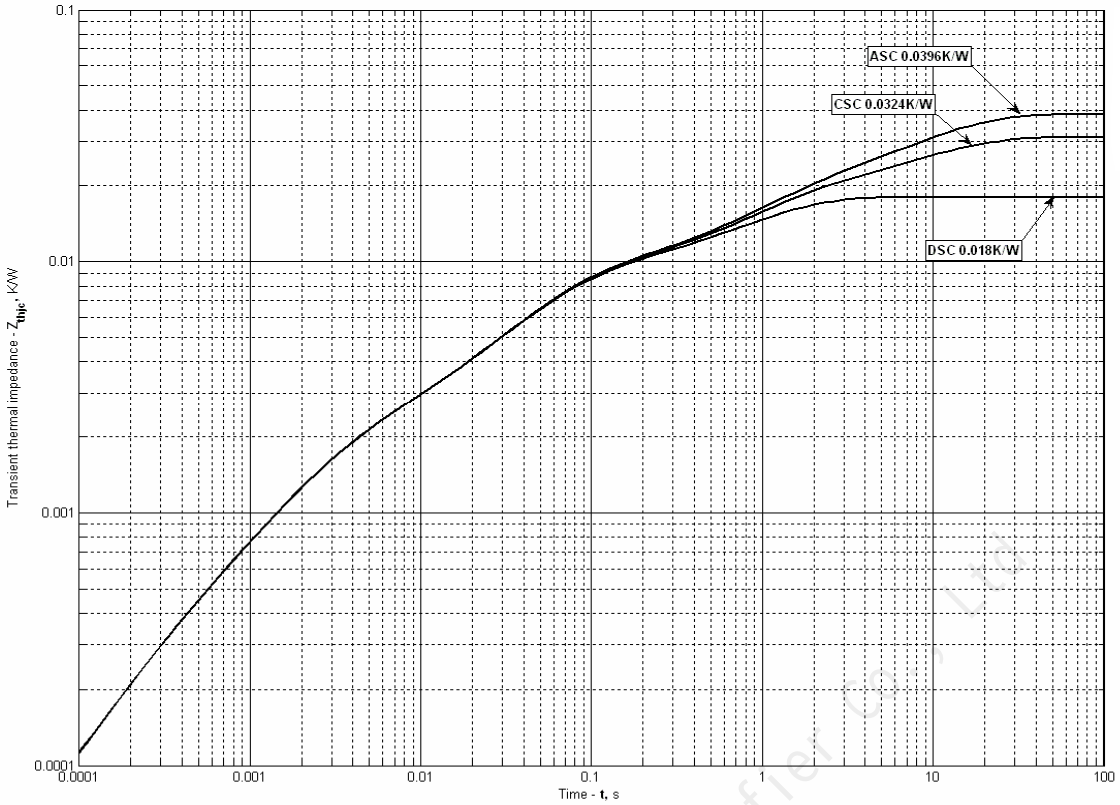


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

$\boldsymbol{\tau_i}$ = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
R_i, K/W	0.009241	0.006037	0.001231	0.001054	0.0003396	0.00009575
τ_i, s	0.9673	0.04967	0.002733	0.07734	0.001638	0.0002248

DC Anode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.01318	0.009281	0.006055	0.001018	0.001535	0.0001182
τ_i, s	9.745	1.028	0.05591	0.03732	0.002468	0.0002687

DC Cathode side cooled

i	1	2	3	4	5	6
R_i, K/W	0.02041	0.009325	0.006949	0.0001252	0.001516	0.0001119
τ_i, s	9.752	1.065	0.05344	0.01407	0.002421	0.0002554

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

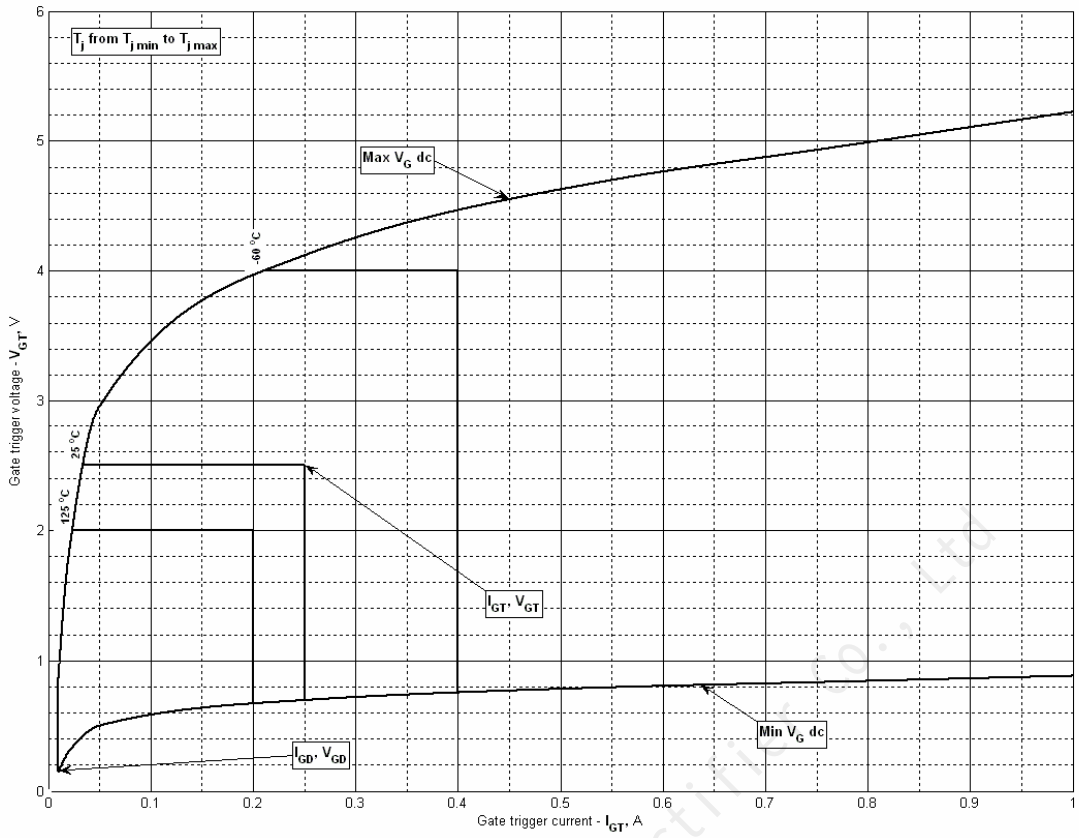


Fig 3 – Gate characteristics – Trigger limits

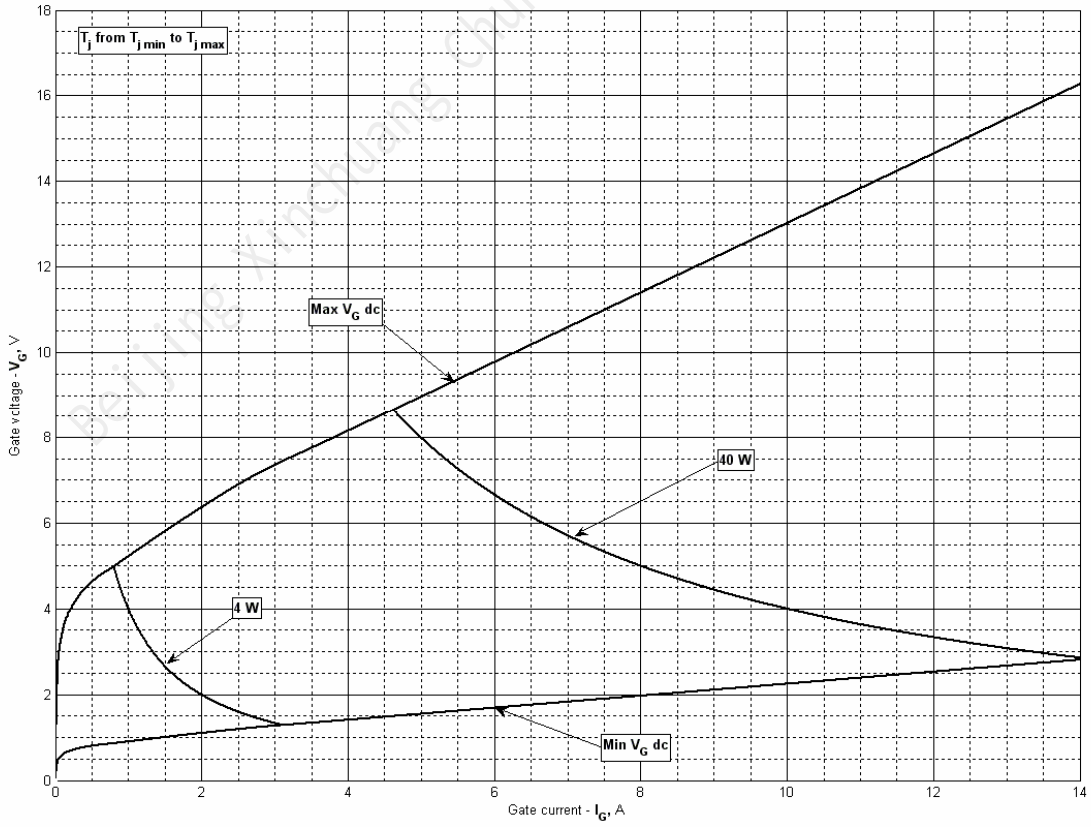


Fig 4 - Gate characteristics –Power curves

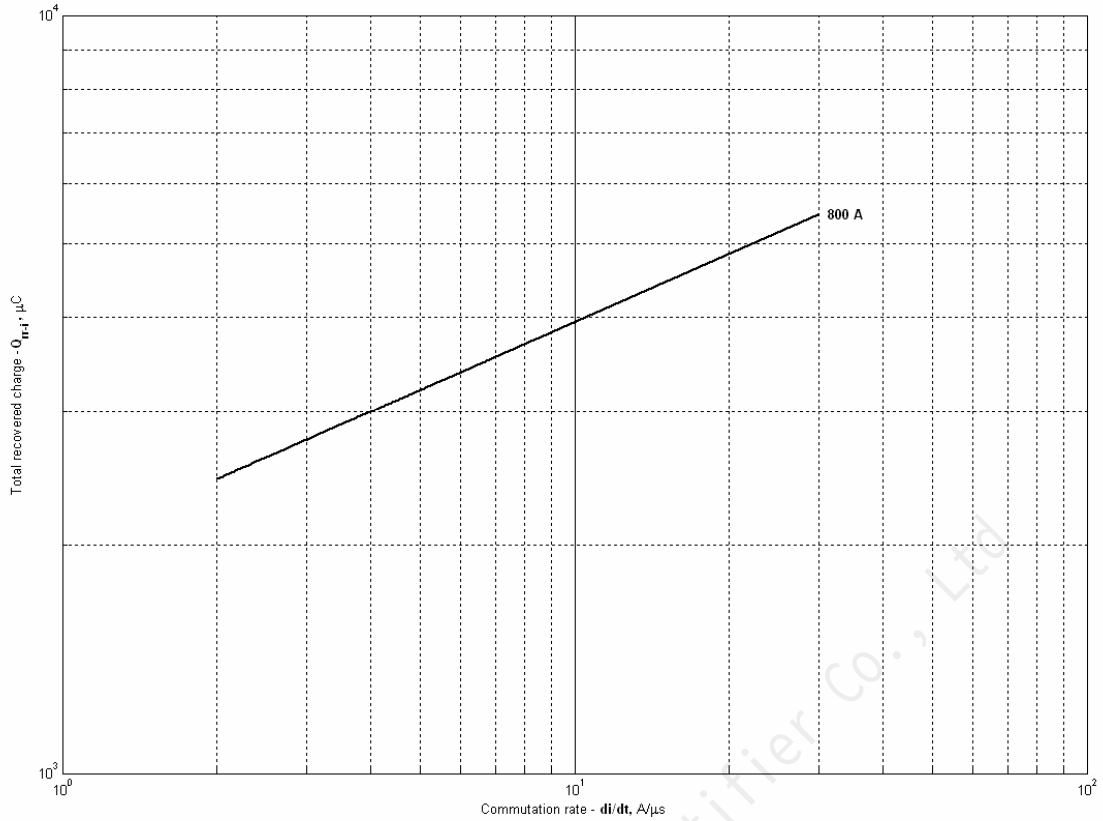


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

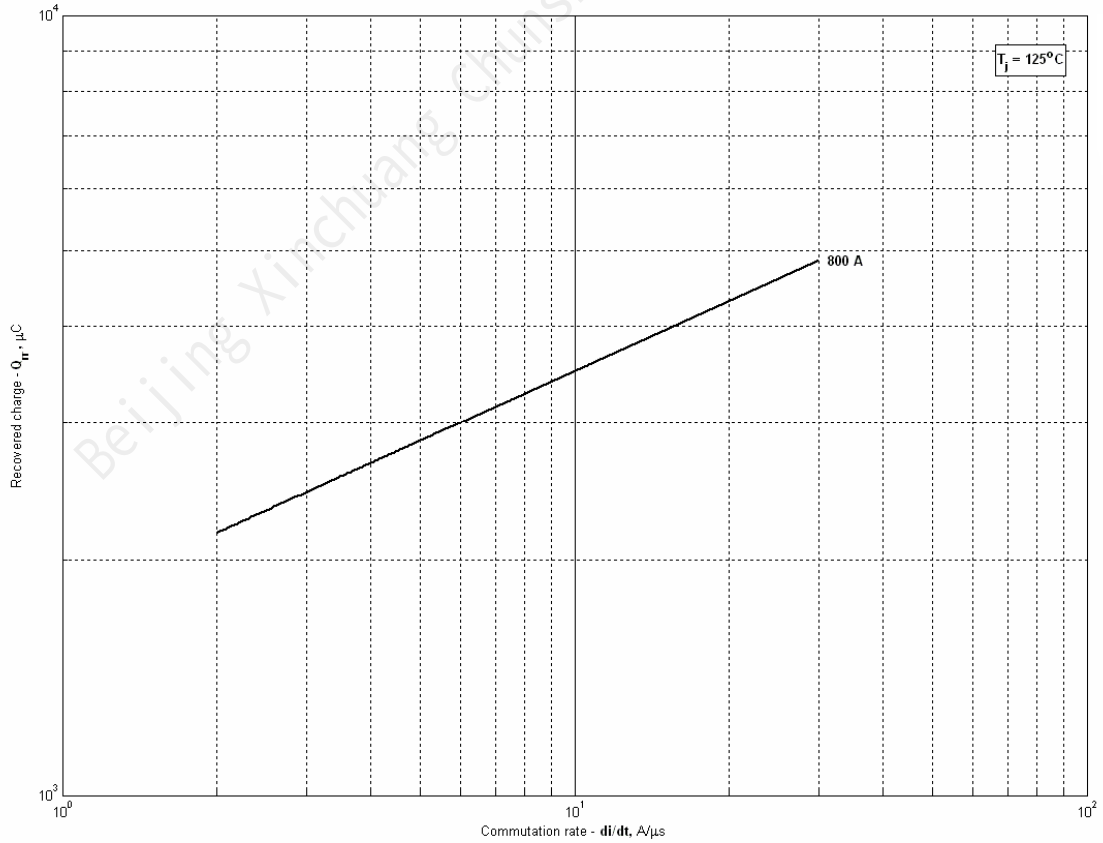


Fig 6 - Recovered charge, Q_{rr} (linear)

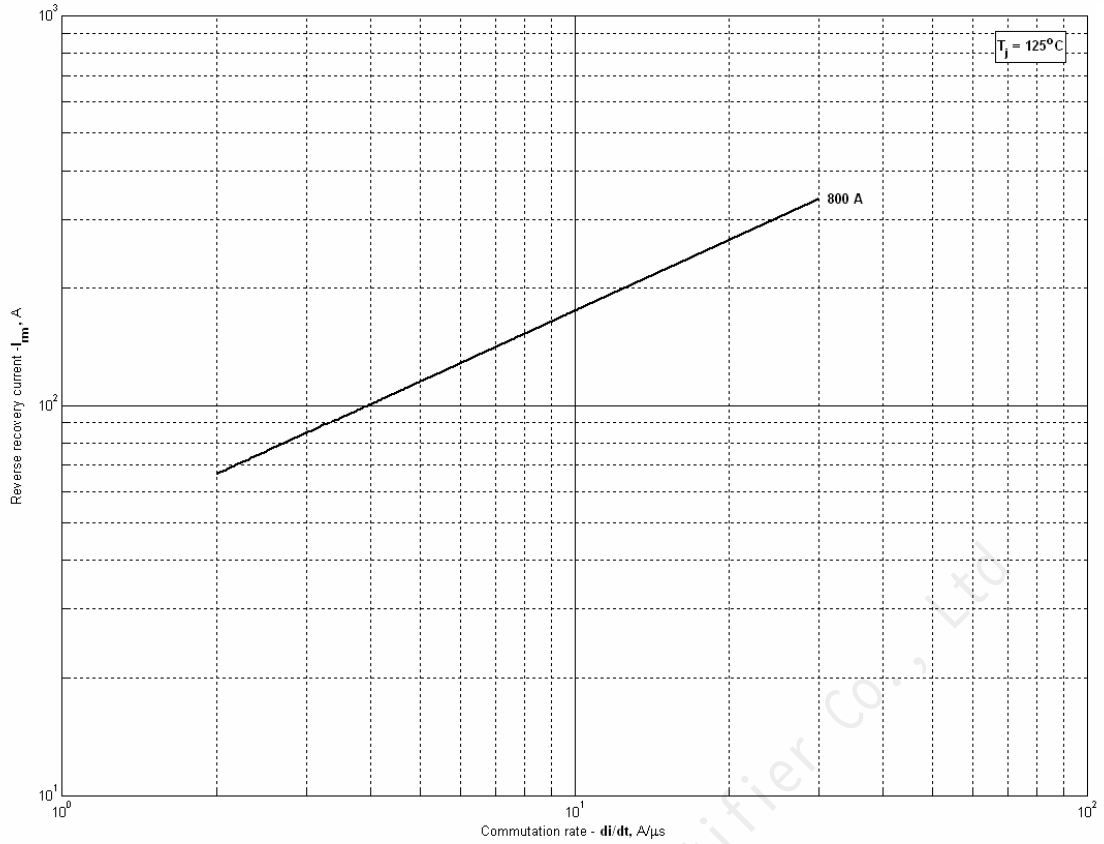


Fig 7 – Peak reverse recovery current, I_{rm}

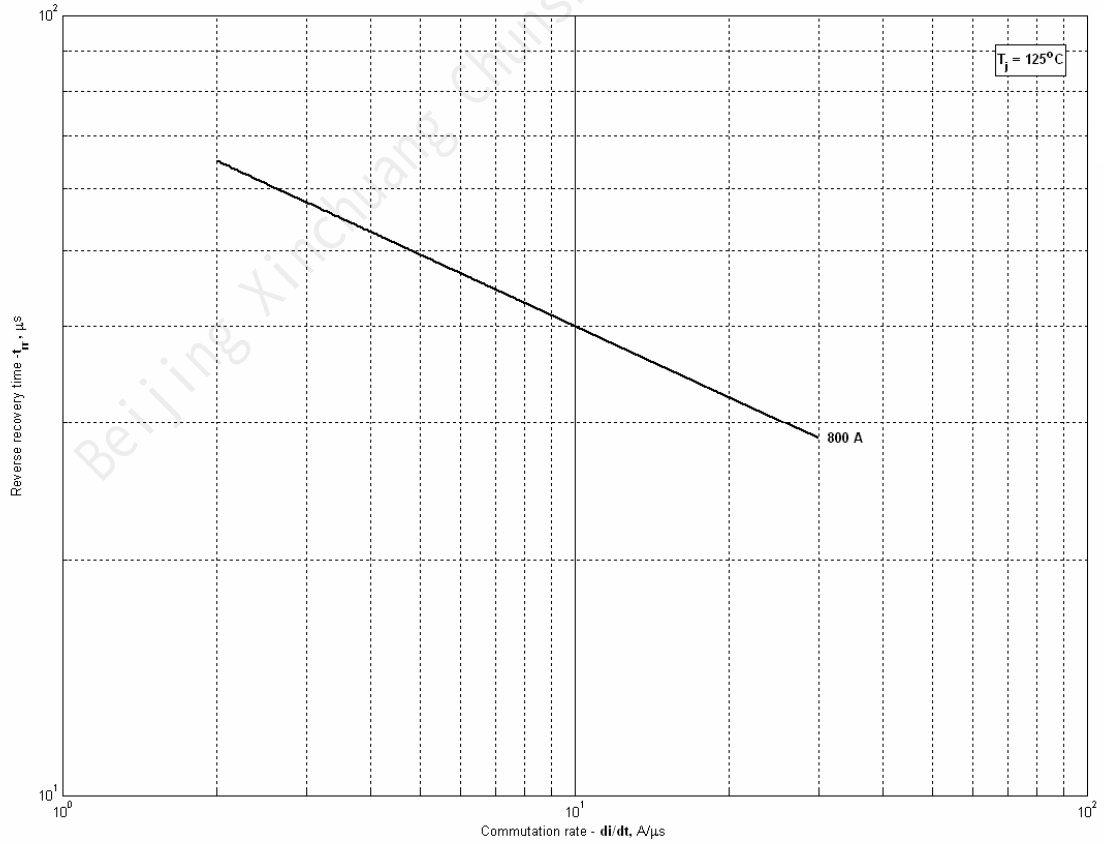


Fig 8 – Maximum recovery time, t_{rr} (linear)

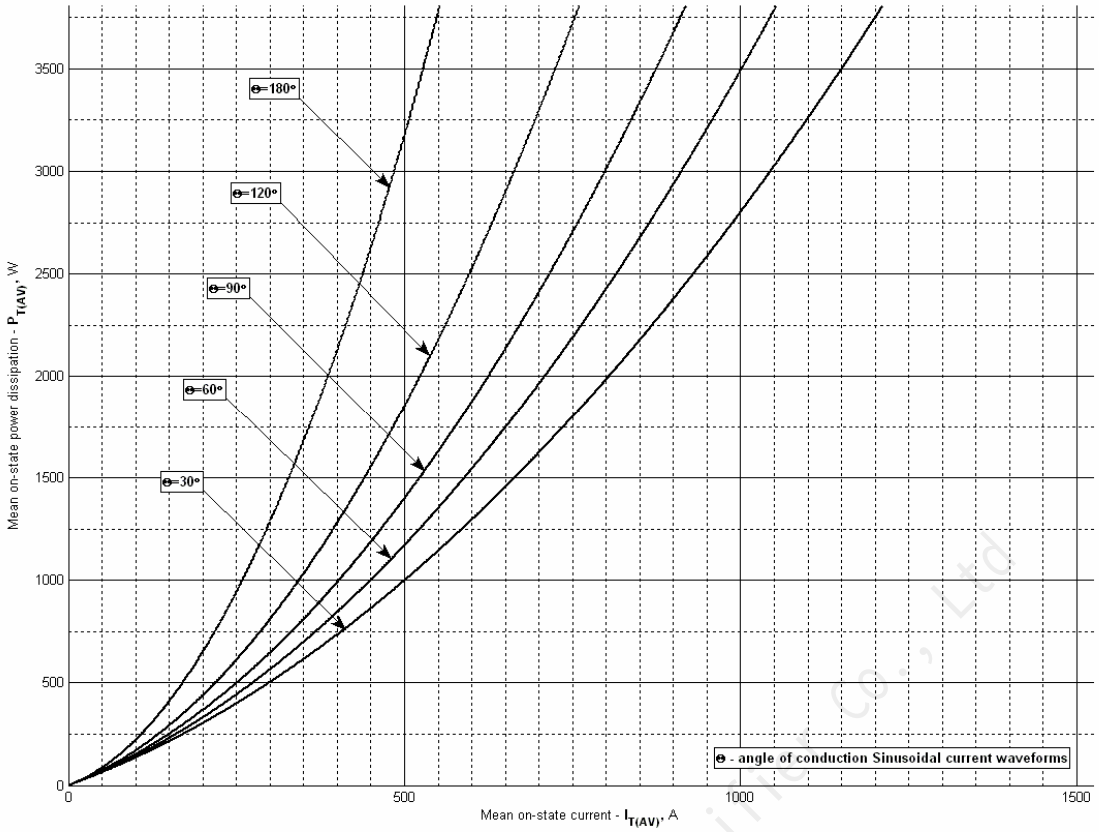


Fig 9 – On-state power loss (sinusoidal current waveforms)

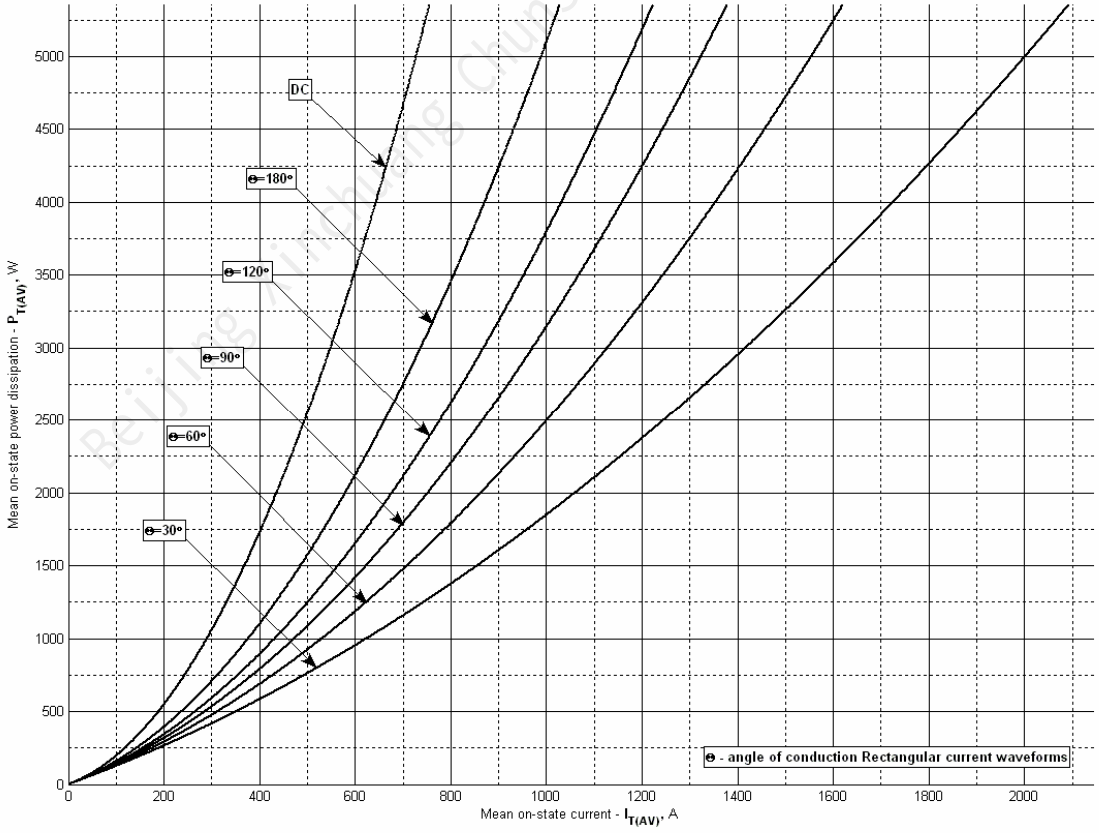


Fig 10 – On-state power loss (rectangular current waveforms)

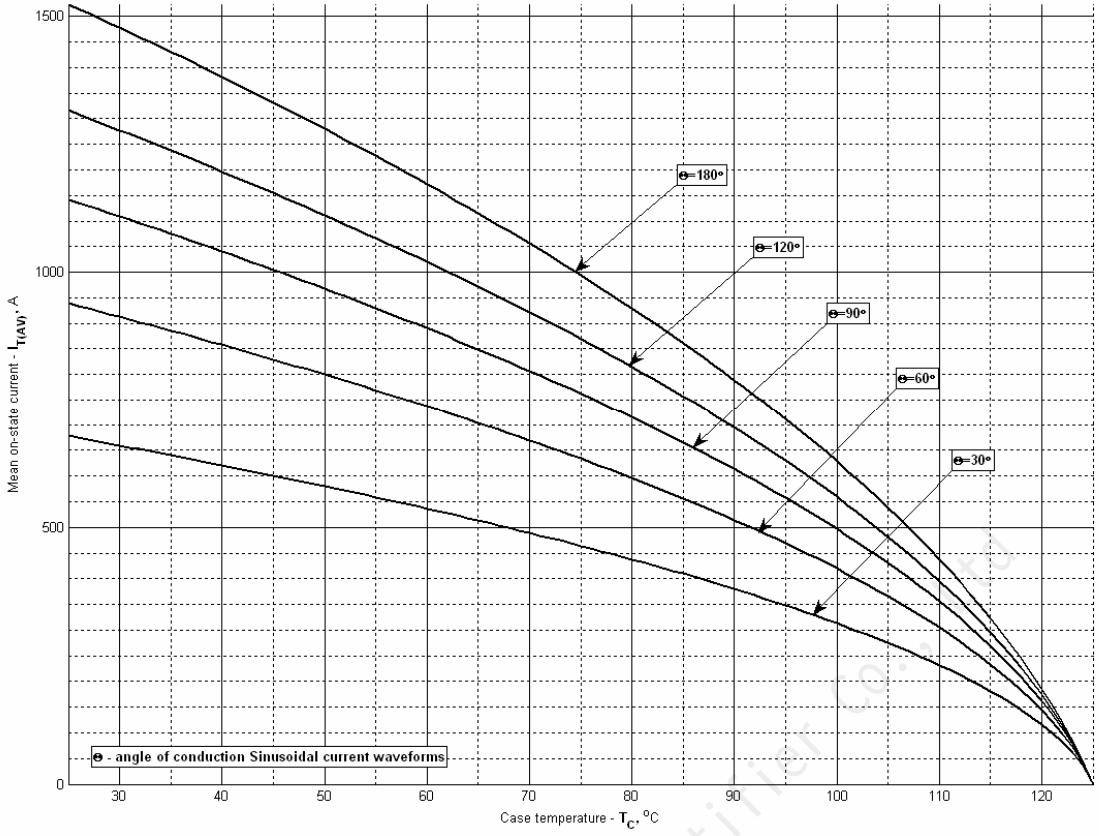


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

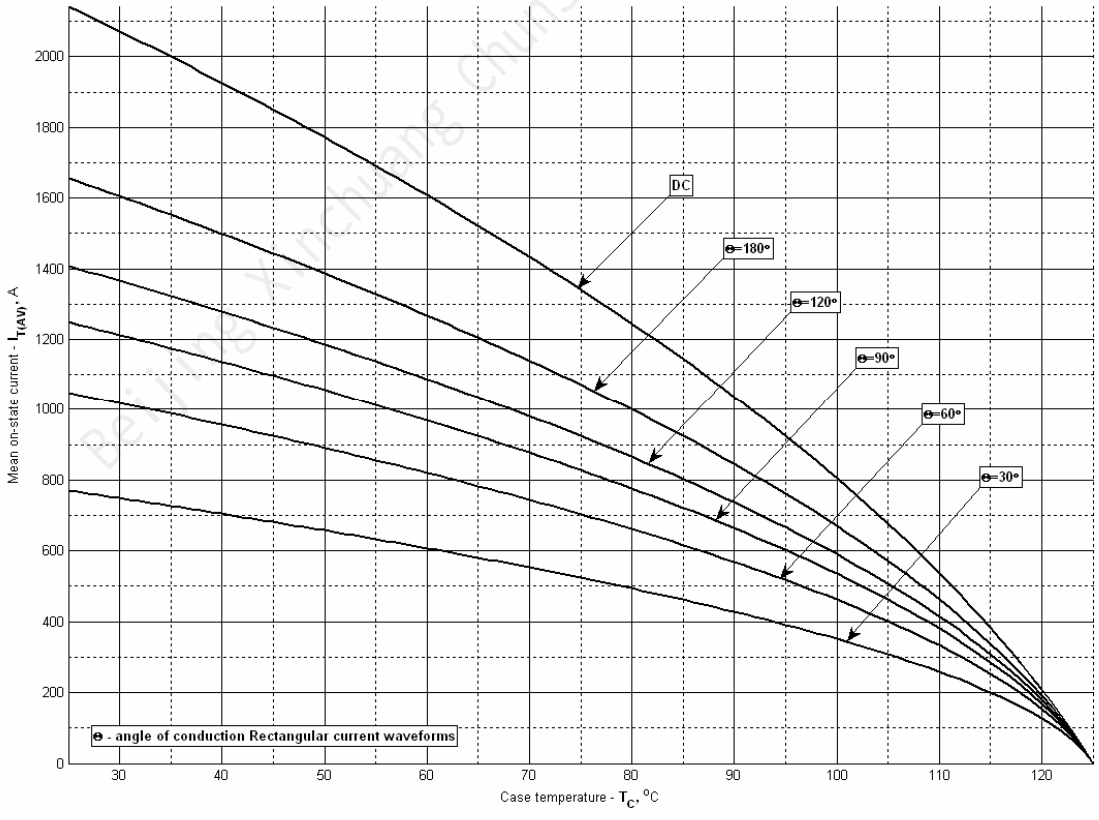


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

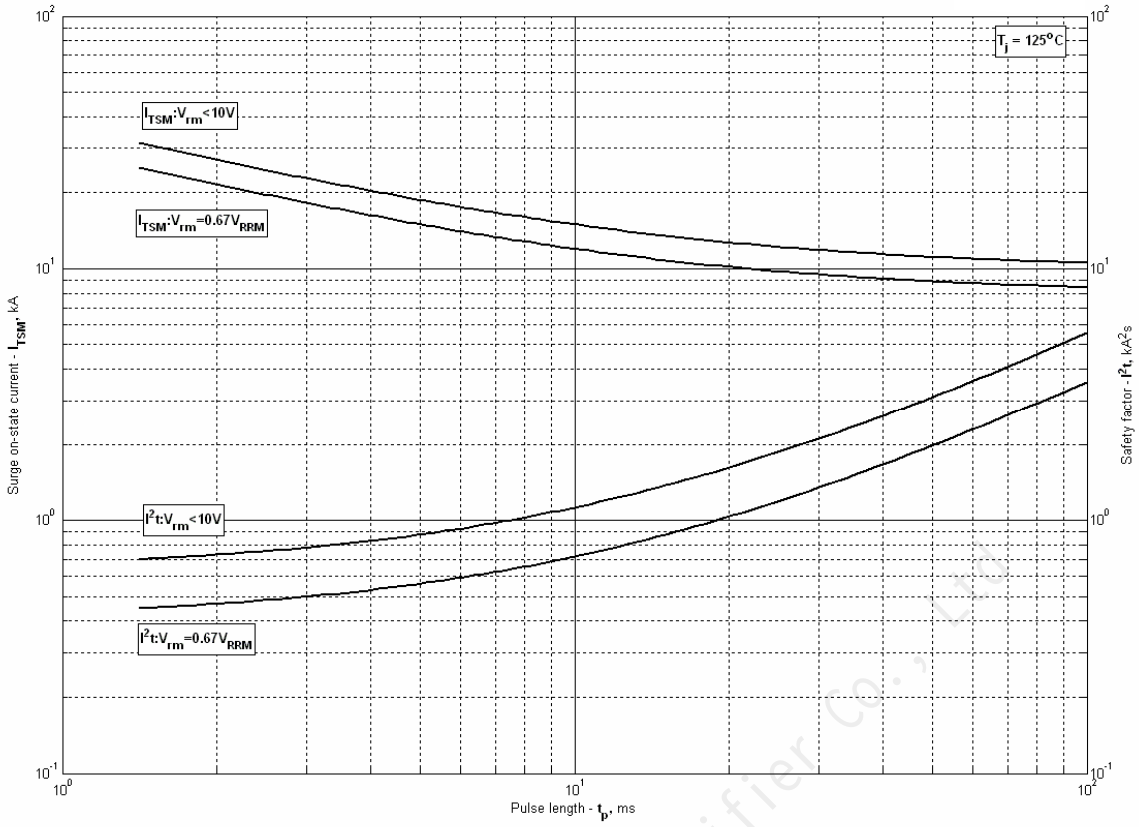


Fig 13 – Maximum surge and I^2t ratings

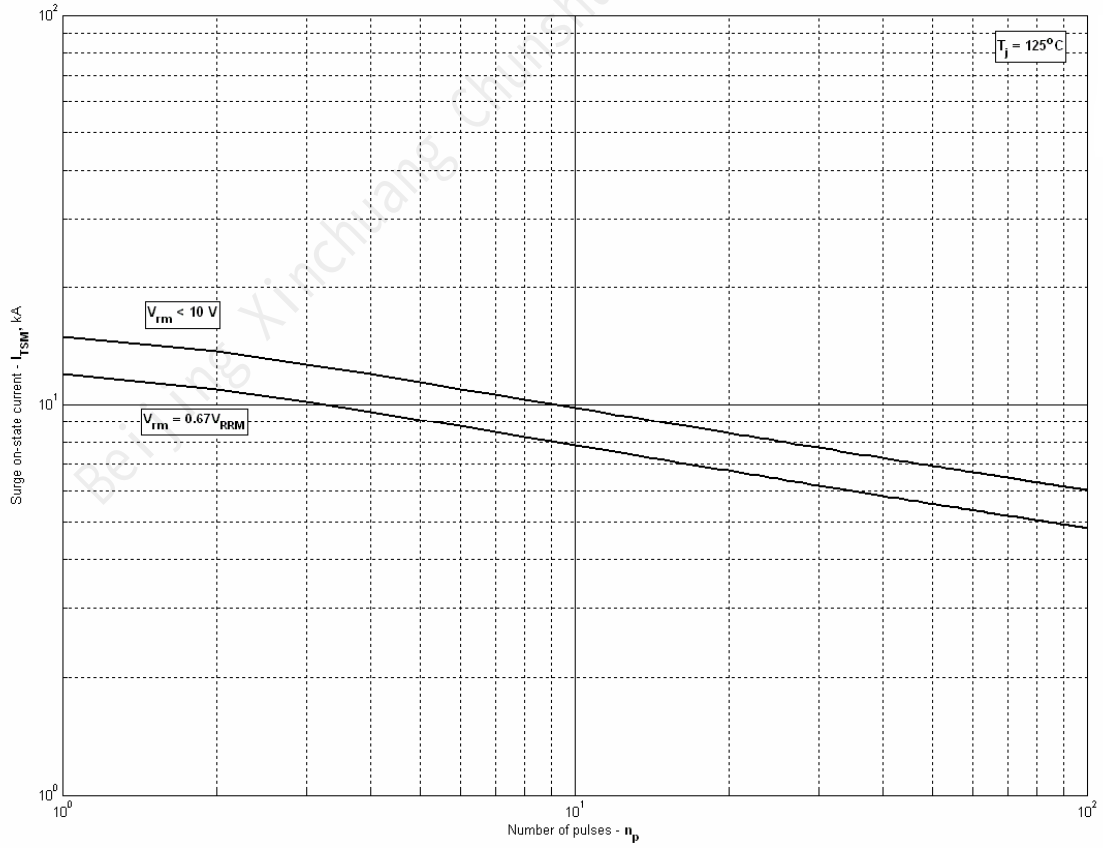


Fig 14 – Maximum surge ratings

