ChunZheng

High-end Power Semiconductor Manufacturer

# KP1600A 5400V-6500V

## Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Mean on-state current | | | $I_{TAV}$ | 1600 A | | | |
| Repetitive peak off-state voltage | | | $V_{DRM}$ | 5400 – 6500 V | | | |
| Repetitive peak reverse voltage | | | $V_{RRM}$ | | | | |
| Turn-off time | | | $t_q$ | 800 µs | | | |
| $V_{DRM}$, $V_{RRM}$, V | 5400 | 5600 | 5800 | 6000 | 6200 | 6400 | 6500 |
| Voltage code | 54 | 56 | 58 | 60 | 62 | 64 | 65 |
| $T_j$, °C | – 60 – 125 | | | | | | |

## MAXIMUM ALLOWABLE RATINGS

| Symbols and parameters | | Units | Values | Test conditions | |
|---|---|---|---|---|---|
| **ON-STATE** | | | | | |
| $I_{TAV}$ | Mean on-state current | A | 1600 | $T_c$= 85 °C, Double side cooled<br>180° half-sine wave; 50 Hz | |
| $I_{TRMS}$ | RMS on-state current | A | 2512 | $T_c$= 85 °C, Double side cooled<br>180° half-sine wave; 50 Hz | |
| $I_{TSM}$ | Surge on-state current | kA | 40.0<br>46.0 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 50 Hz<br>($t_p$=10 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse: $I_G$=2 A;<br>$t_{GP}$=50 µs; $di_G/dt$≥1 A/µs |
| | | | 42.0<br>48.0 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 60 Hz<br>($t_p$=8.3 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse: $I_G$=2 A;<br>$t_{GP}$=50 µs; $di_G/dt$≥1 A/µs |
| $I^2t$ | Safety factor | $A^2s{\cdot}10^3$ | 8000<br>10580 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 50 Hz<br>($t_p$=10 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse: $I_G$=2 A;<br>$t_{GP}$=50 µs; $di_G/dt$≥1 A/µs |
| | | | 7320<br>9560 | $T_j$=$T_{j\,max}$<br>$T_j$=25 °C | 180° half-sine wave; 60 Hz<br>($t_p$=8.3 ms); single pulse;<br>$V_D$=$V_R$=0 V;<br>Gate pulse: $I_G$=2 A;<br>$t_{GP}$=50 µs; $di_G/dt$≥1 A/µs |
| **BLOCKING** | | | | | |
| $V_{DRM}$, $V_{RRM}$ | Repetitive peak off-state and<br>Repetitive peak reverse voltages | V | 5400–6500 | $T_{j\,min}$< $T_j$ <$T_{j\,max}$;<br>180° half-sine wave; 50 Hz;<br>Gate open | |
| $V_{DSM}$, $V_{RSM}$ | Non-repetitive peak off-state and<br>Non-repetitive peak reverse voltages | V | 5500–6600 | $T_{j\,min}$< $T_j$ <$T_{j\,max}$;<br>180° half-sine wave; 50 Hz;single pulse;<br>Gate open | |
| $V_D$, $V_R$ | Direct off-state and<br>Direct reverse voltages | V | 0.75·$V_{DRM}$<br>0.75·$V_{RRM}$ | $T_j$=$T_{j\,max}$;<br>Gate open | |

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|---|---|---|---|---|
| **TRIGGERING** | | | | |
| $I_{FGM}$ | Peak forward gate current | A | 10 | $T_j=T_{j\,max}$ |
| $V_{RGM}$ | Peak reverse gate voltage | V | 5 | |
| $P_G$ | Gate power dissipation | W | 5 | $T_j=T_{j\,max}$ for DC gate current |
| **SWITCHING** | | | | |
| $(di_T/dt)_{crit}$ | Critical rate of rise of on-state current non-repetitive (f=1 Hz) | A/μs | 630 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs |
| **THERMAL** | | | | |
| $T_{stg}$ | Storage temperature | °C | -60 – 125 | |
| $T_j$ | Operating junction temperature | °C | -60 – 125 | |
| **MECHANICAL** | | | | |
| F | Mounting force | kN | 60.0 – 70.0 | |
| a | Acceleration | $m/s^2$ | 50<br>100 | Device unclamped<br>Device clamped |

## CHARACTERISTICS

| Symbols and parameters | | Units | Values | Conditions | |
|---|---|---|---|---|---|
| **ON-STATE** | | | | | |
| $V_{TM}$ | Peak on-state voltage, max | V | 2.80 | $T_j=25$ °C; $I_{TM}=6300$ A | |
| $V_{T(TO)}$ | On-state threshold voltage, max | V | 1.10 | $T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$ | |
| $r_T$ | On-state slope resistance, max | mΩ | 0.350 | | |
| $I_L$ | Latching current, max | mA | 1500 | $T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs | |
| $I_H$ | Holding current, max | mA | 300 | $T_j=25$ °C; $V_D=12$ V; Gate open | |
| **BLOCKING** | | | | | |
| $I_{DRM}$, $I_{RRM}$ | Repetitive peak off-state and Repetitive peak reverse currents, max | mA | 200 | $T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$ | |
| $(dv_D/dt)_{crit}$ | Critical rate of rise of off-state voltage[1)], min | V/μs | 1000 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open | |
| **TRIGGERING** | | | | | |
| $V_{GT}$ | Gate trigger direct voltage, max | V | 3.00<br>2.00 | $T_j=25$ °C<br>$T_j=T_{j\,max}$ | $V_D=12$ V; $I_D=3$ A; Direct gate current |
| $I_{GT}$ | Gate trigger direct current, max | mA | 300<br>200 | $T_j=25$ °C<br>$T_j=T_{j\,max}$ | |
| $V_{GD}$ | Gate non-trigger direct voltage, min | V | 0.35 | $T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current | |
| $I_{GD}$ | Gate non-trigger direct current, min | mA | 15.00 | | |
| **SWITCHING** | | | | | |
| $t_{gd}$ | Delay time | μs | 4.00 | $T_j=25$ °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs | |
| $t_q$ | Turn-off time[2)], max | μs | 800 | $dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=2000$ A; $di_R/dt=-10$ A/μs; $V_R=100$ V; $V_D=0.67\ V_{DRM}$ | |
| $Q_{rr}$ | Total recovered charge, max | μC | 7600 | $T_j=T_{j\,max}$; $I_{TM}=2000$ A; $di_R/dt=-5$ A/μs; $V_R=100$ V | |
| $t_{rr}$ | Reverse recovery time, typ | μs | 80 | | |
| $I_{rrM}$ | Peak reverse recovery current, max | A | 190 | | |



 

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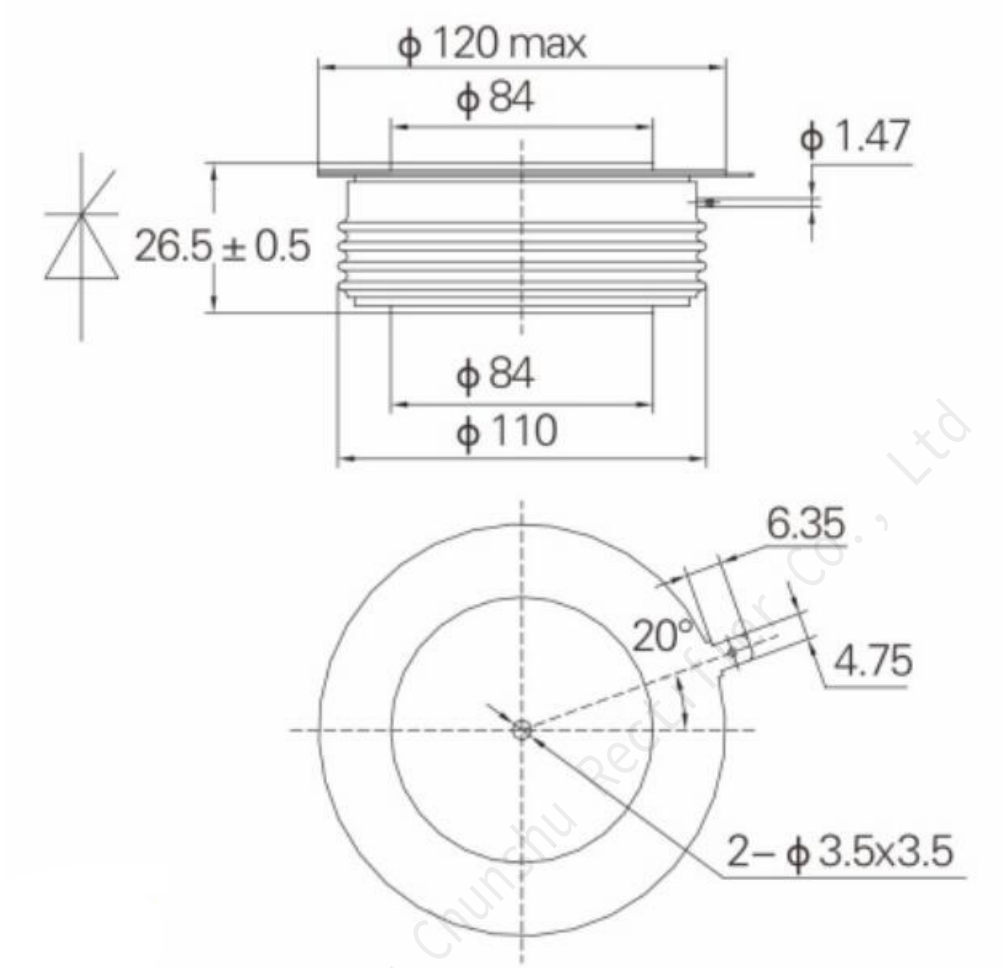
|---|---|---|---|---|---|
| **THERMAL** | | | | | |
| $R_{thjc}$ | Thermal resistance, junction to case, max | °C/W | 0.0065 | Direct current | Double side cooled |
| $R_{thjc-A}$ | | | 0.0143 | | Anode side cooled |
| $R_{thjc-K}$ | | | 0.0117 | | Cathode side cooled |
| $R_{thck}$ | Thermal resistance, case to heatsink, max | °C/W | 0.0015 | Direct current | |
| **MECHANICAL** | | | | | |
| w | Weight, typ | g | 1900 | | |
| $D_s$ | Surface creepage distance | mm (inch) | 36.50 (1.437) | | |
| $D_a$ | Air strike distance | mm (inch) | 16.5 (0.650) | | |



## OVERALL DIMENSIONS




KT90

All dimensions in millimeters



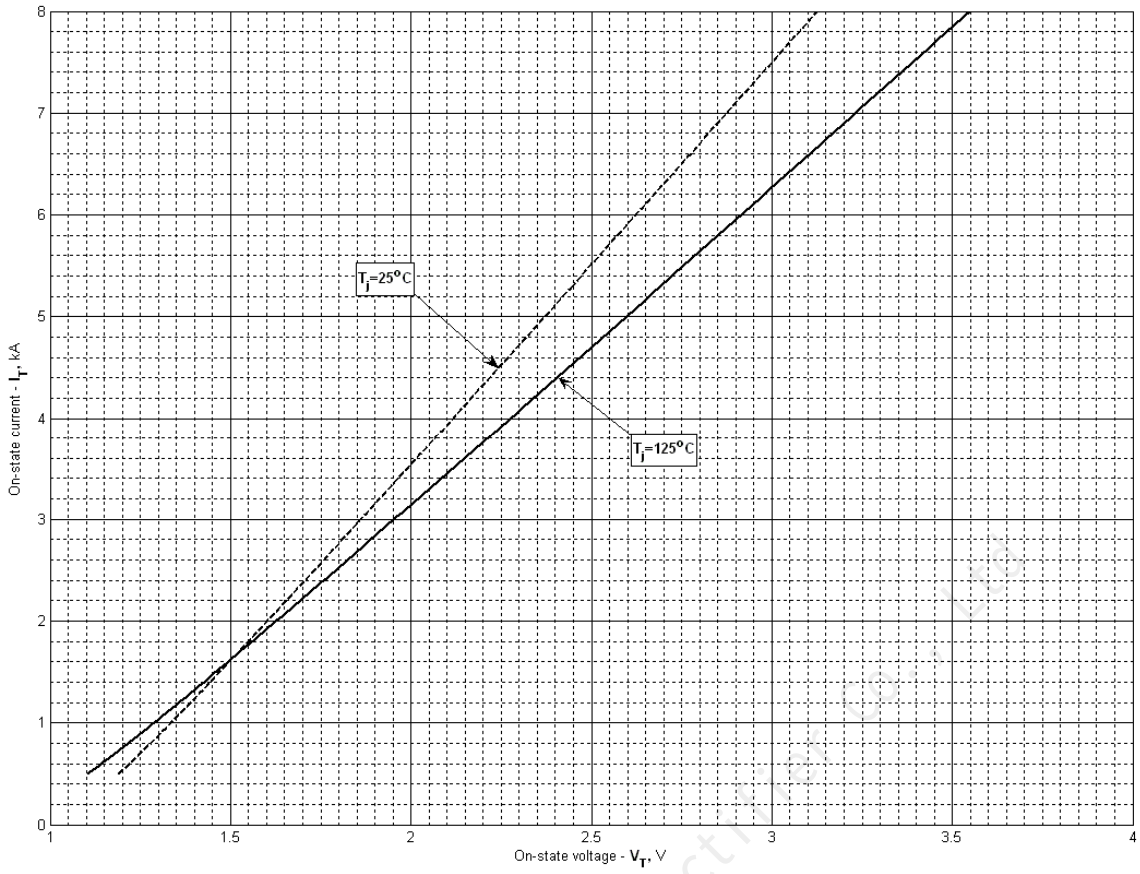



**Fig 1 – On-state characteristics of Limit device**

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

| | Coefficients for max curves | |
|---|---|---|
| | $T_j$ = 25°C | $T_j = T_{j\,max}$ |
| **A** | 0.913434 | 0.744654 |
| **B** | 0.208728 | 0.259885 |
| **C** | -0.253813 | -0.338985 |
| **D** | 0.388412 | 0.518752 |

**On-state characteristic model (see Fig. 1)**



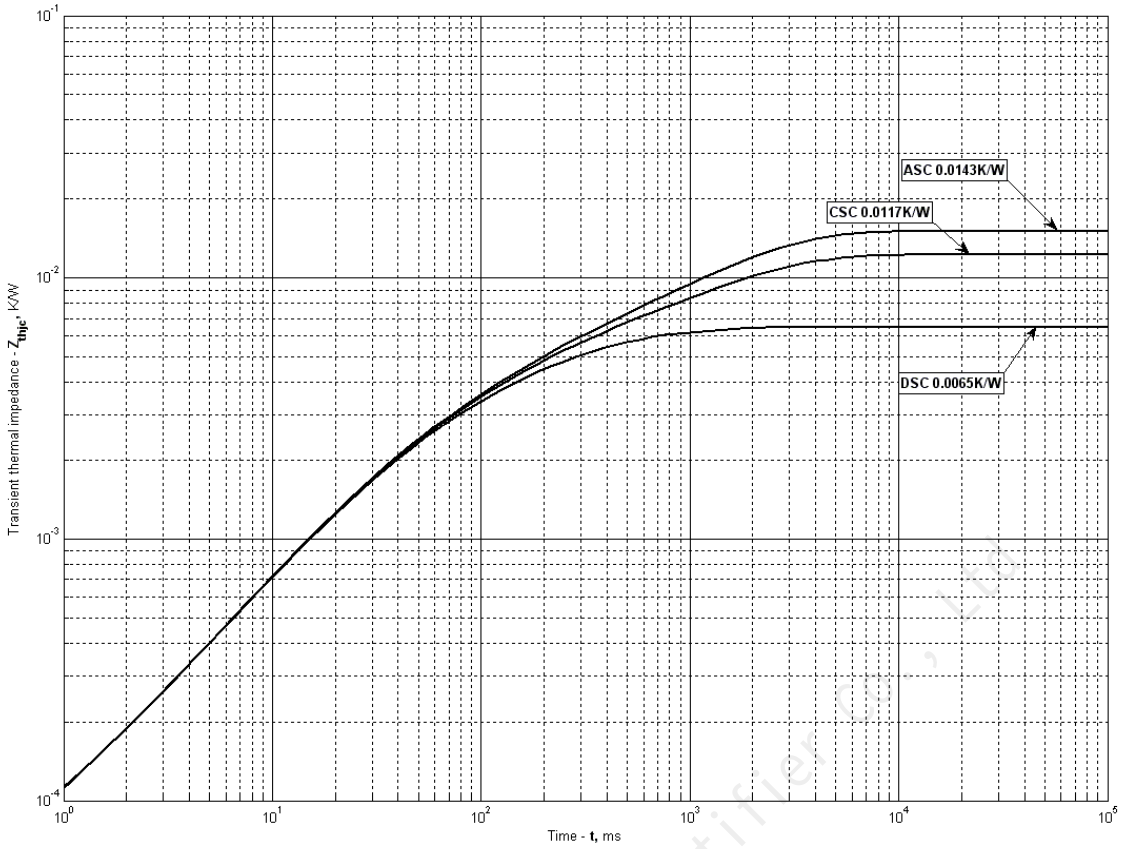



**Fig 2 – Transient thermal impedance**

Analytical function for Transient thermal impedance junction to case $Z_{thjc}$ for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left( 1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

**t** = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of $p_{th}$ term.

$\boldsymbol{\tau_i}$ = Time constatnt of $r_{th}$ term.

DC Double side cooled

| i | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $\mathbf{R_i}$, **K/W** | 0.001031 | 0.003117 | 0.001895 | 0.0004176 | 2.061e-005 | 1.999e-005 |
| $\boldsymbol{\tau_i}$, **s** | 0.7345 | 0.209 | 0.05291 | 0.01652 | 0.0006764 | 0.0002168 |

DC Cathode side cooled

| i | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $\mathbf{R_i}$, **K/W** | 0.001475 | 0.005797 | 0.002722 | 0.001822 | 0.0003923 | 3.824e-005 |
| $\boldsymbol{\tau_i}$, **s** | 0.8755 | 1.835 | 0.1997 | 0.05221 | 0.01594 | 0.0003499 |

DC Anode side cooled

| i | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $\mathbf{R_i}$, **K/W** | 0.00848 | 0.001792 | 0.002597 | 0.00179 | 0.0003904 | 3.851e-005 |
| $\boldsymbol{\tau_i}$, **s** | 1.845 | 0.9581 | 0.2011 | 0.05234 | 0.01605 | 0.0003606 |

**Transient thermal impedance junction to case $\mathbf{Z_{thjc}}$ model (see Fig. 2)**

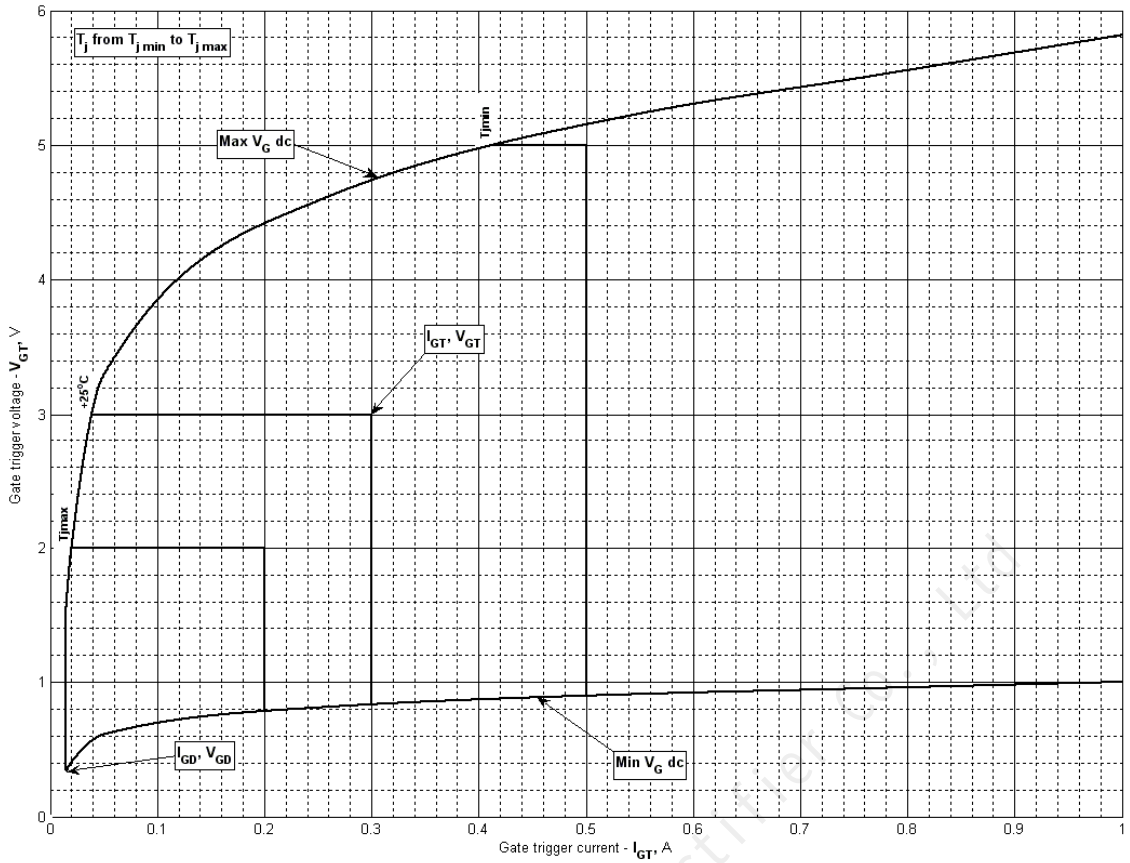



**Fig 3 – Gate characteristics – Trigger limits**

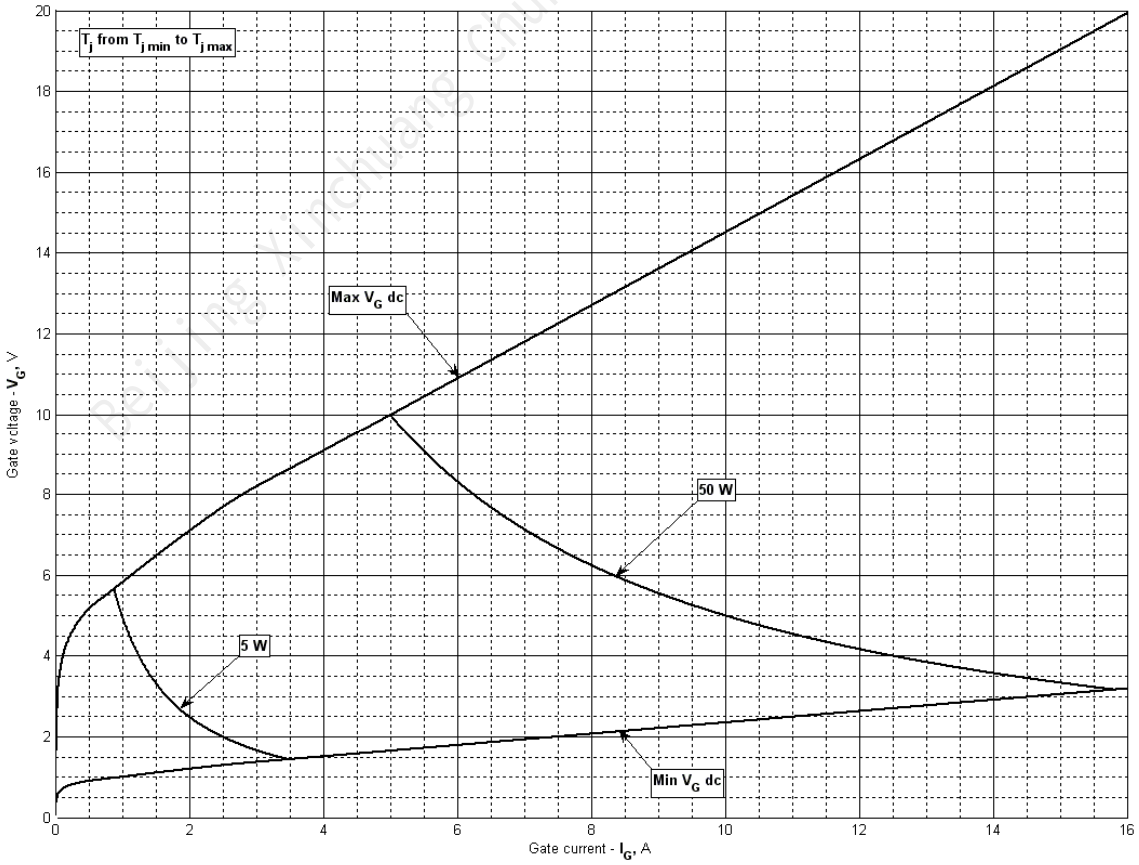



**Fig 4 - Gate characteristics –Power curves**

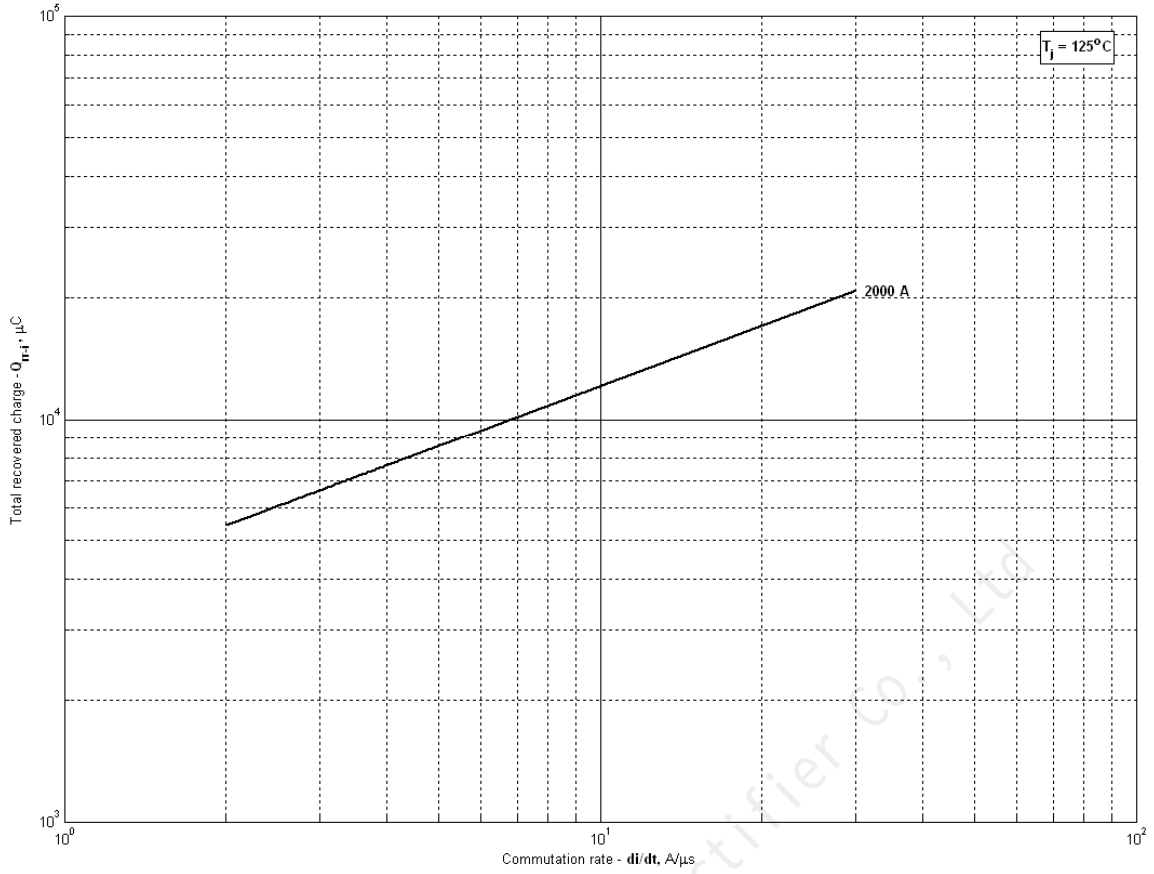



**Fig 5 – Total recovered charge, $Q_{rr-i}$ (integral)**


**Fig 6 - Recovered charge, $Q_{rr}$ (linear)**



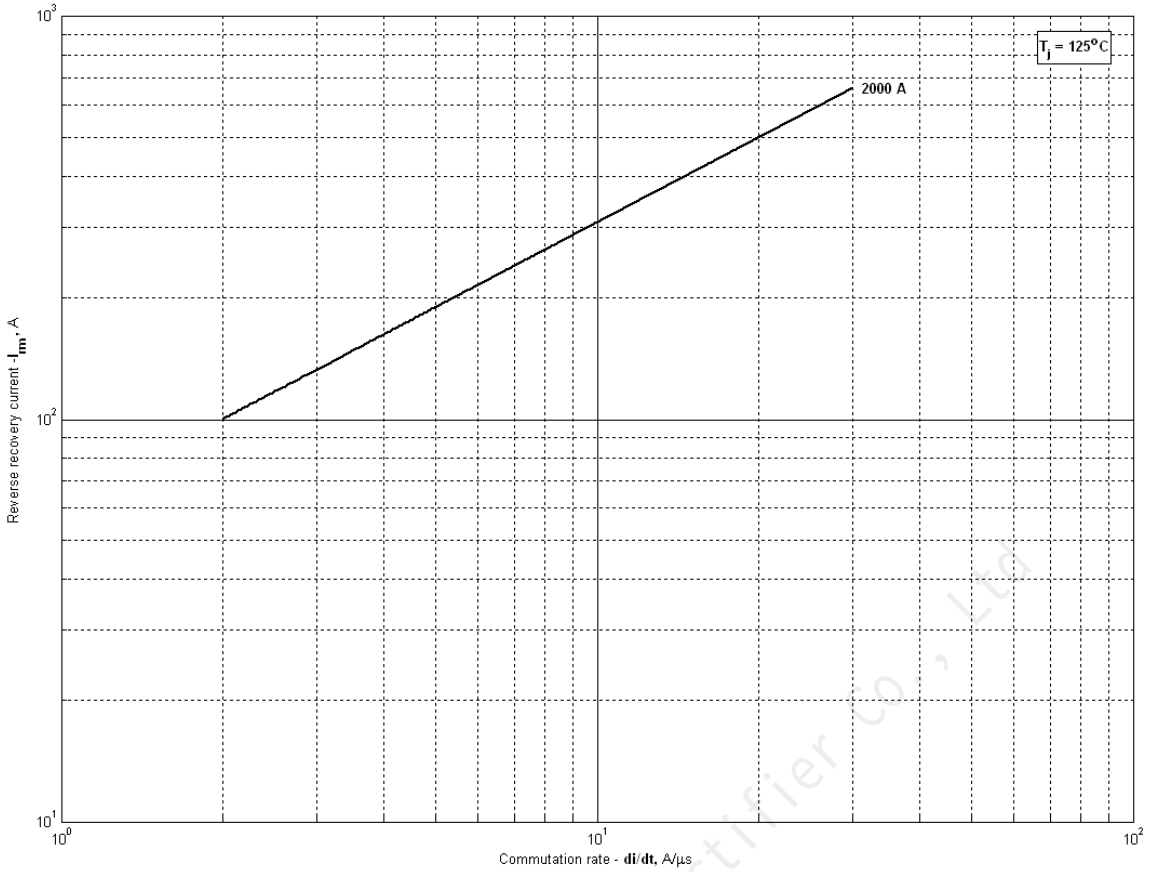



**Fig 7 – Peak reverse recovery current, $I_{rm}$**

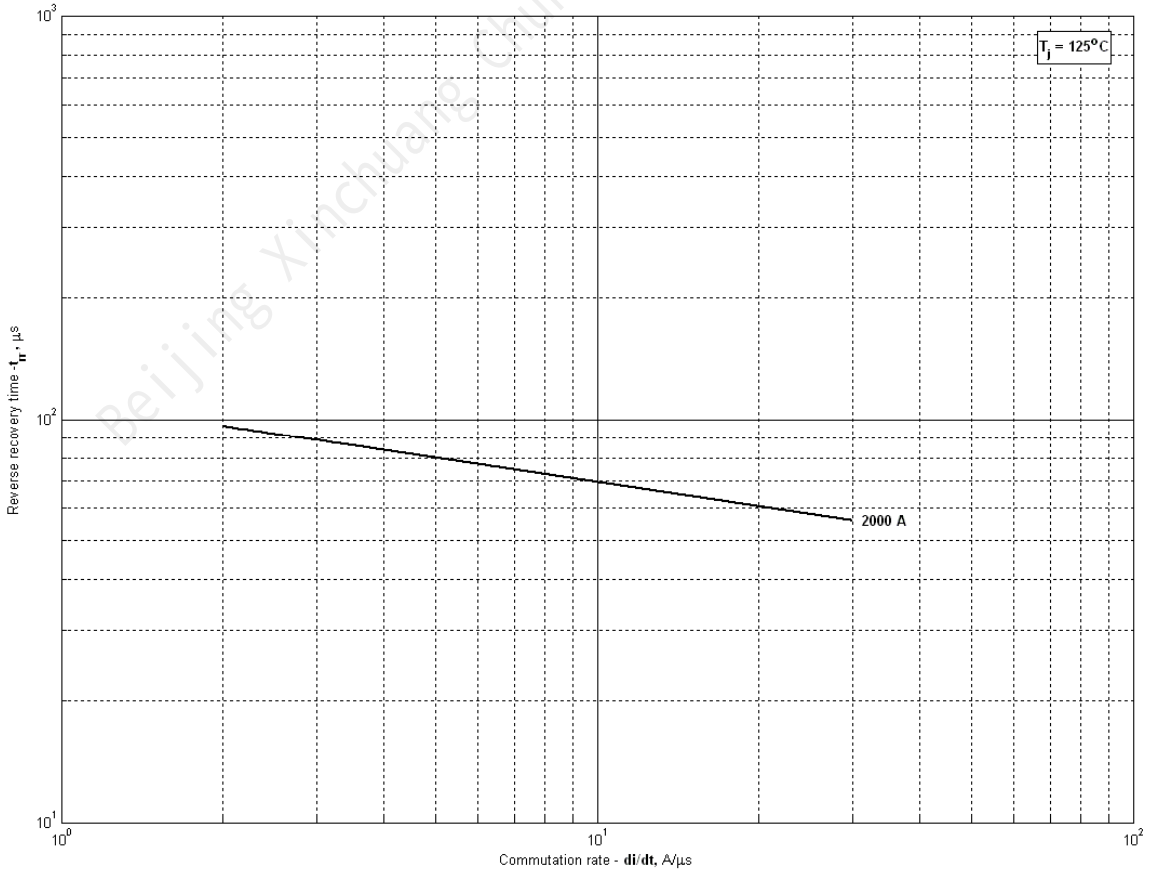



**Fig 8 – Maximum recovery time, $t_{rr}$ (linear)**



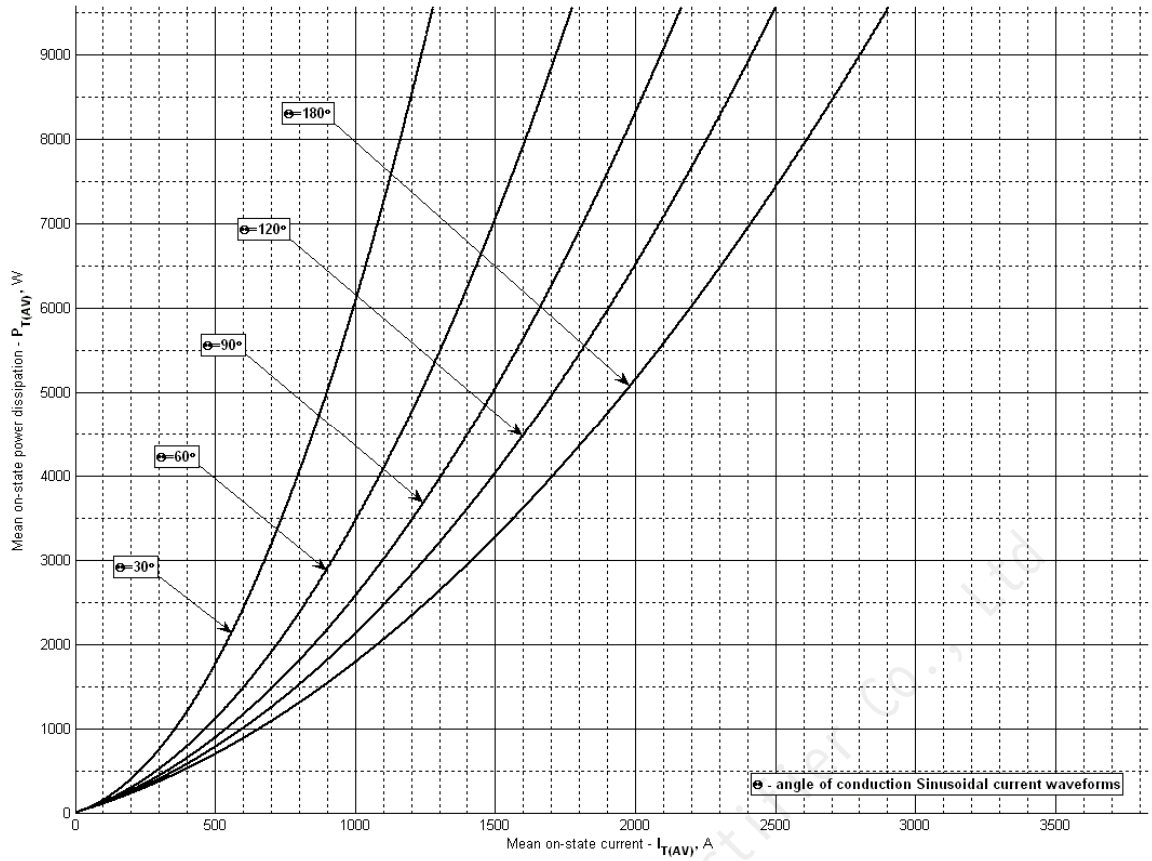



**Fig 9 – On-state power loss (sinusoidal current waveforms)**

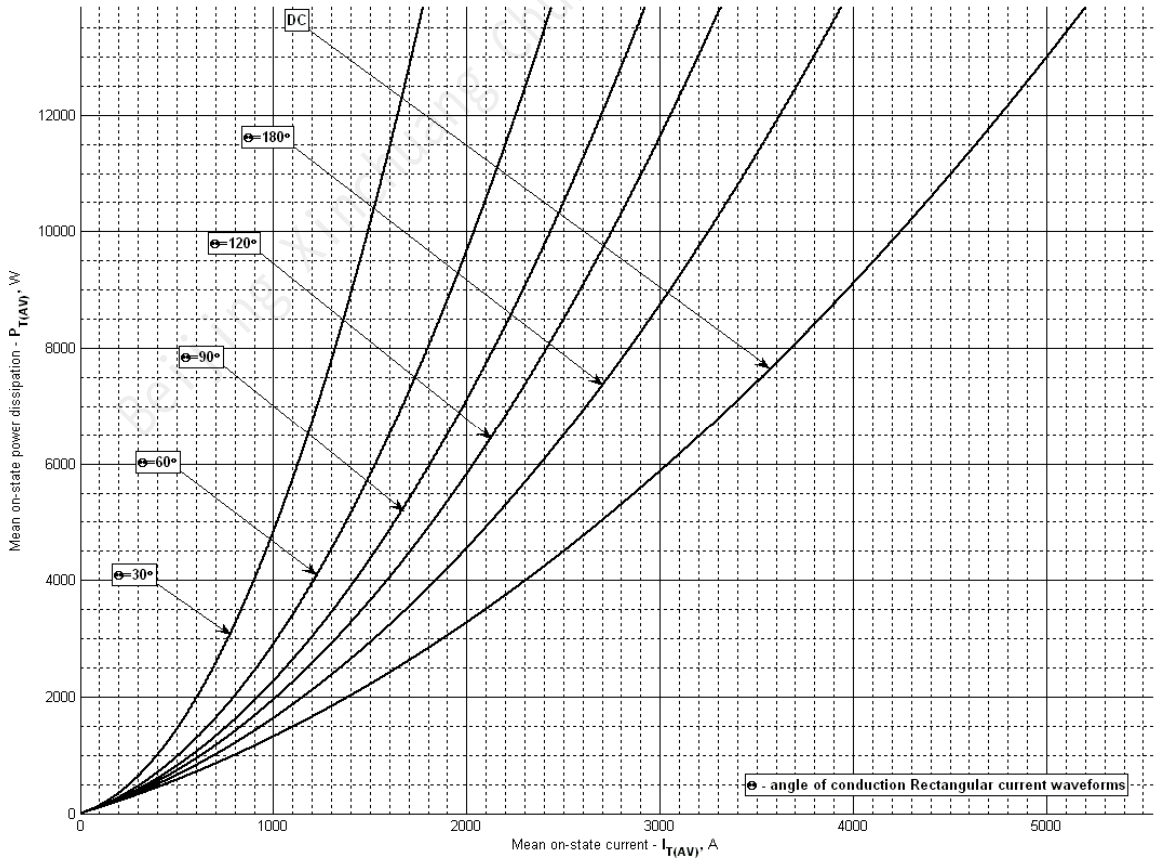



**Fig 10 – On-state power loss (rectangular current waveforms)**

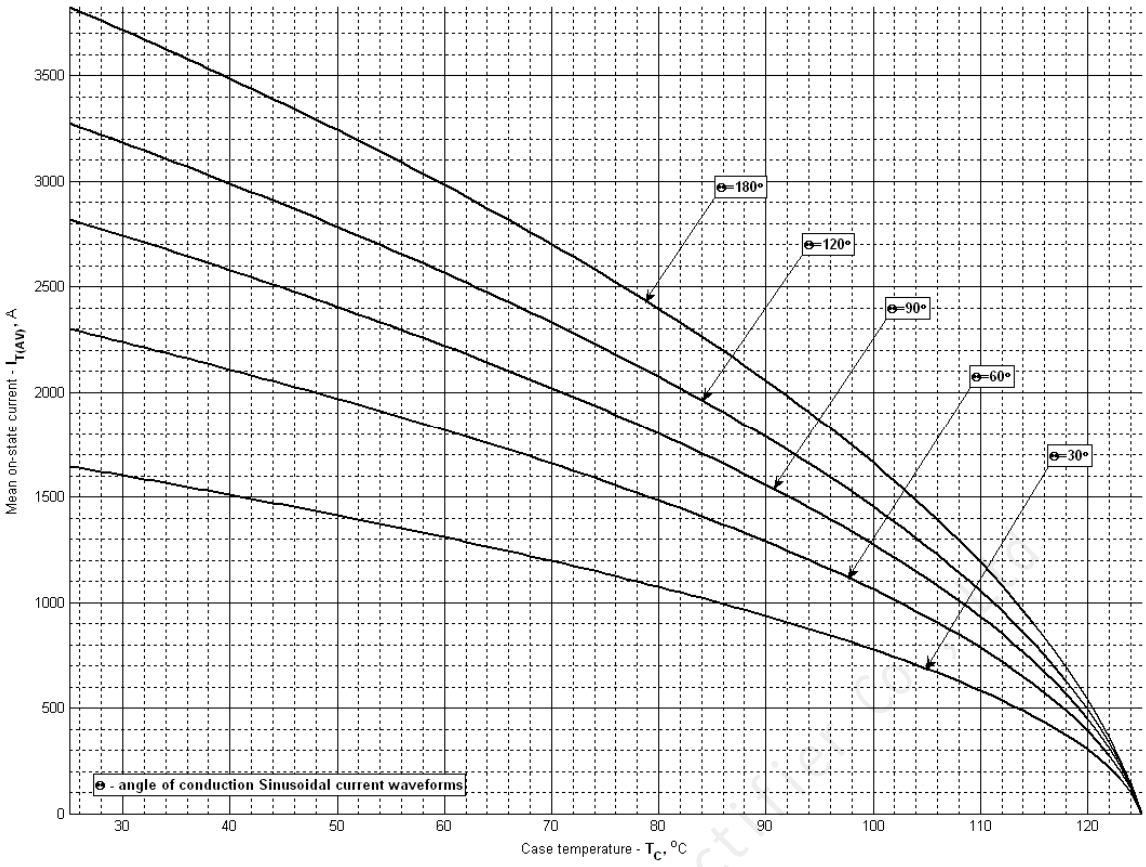



**Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)**

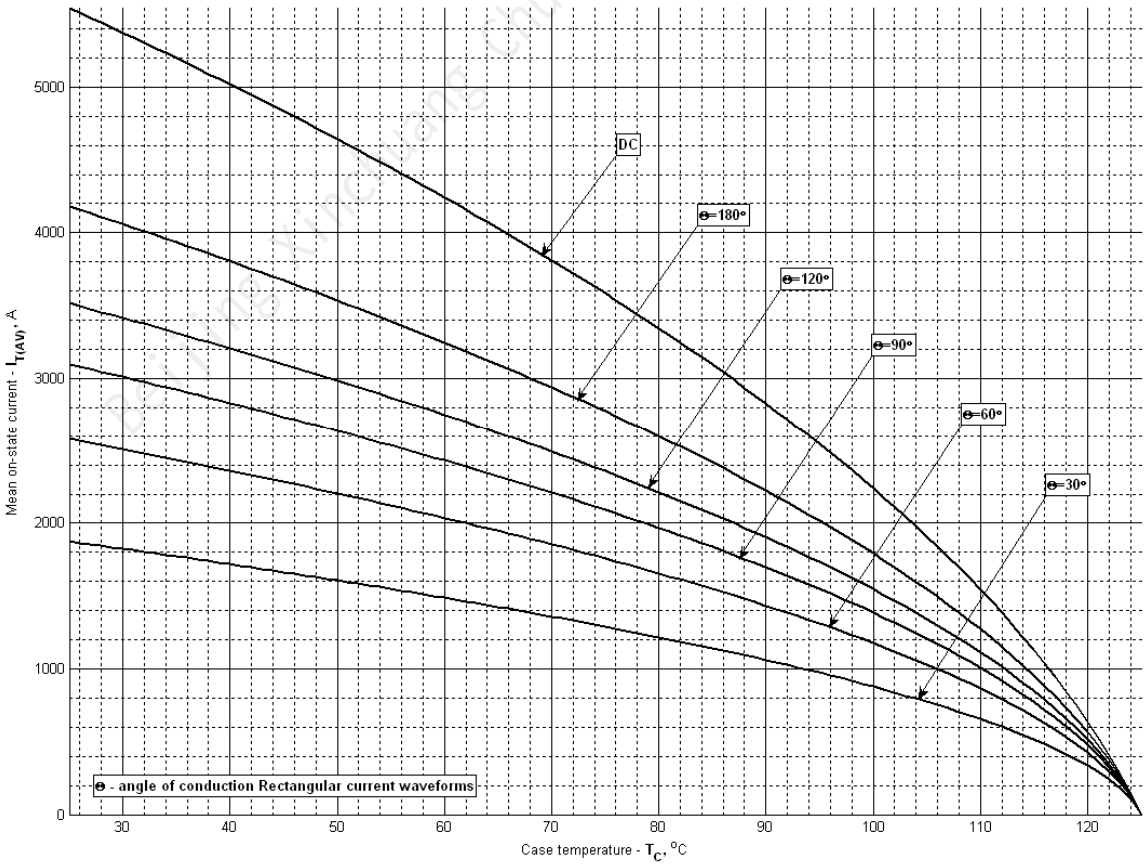



**Fig 12 – Maximum case temperature DSC (rectangular current waveforms)**

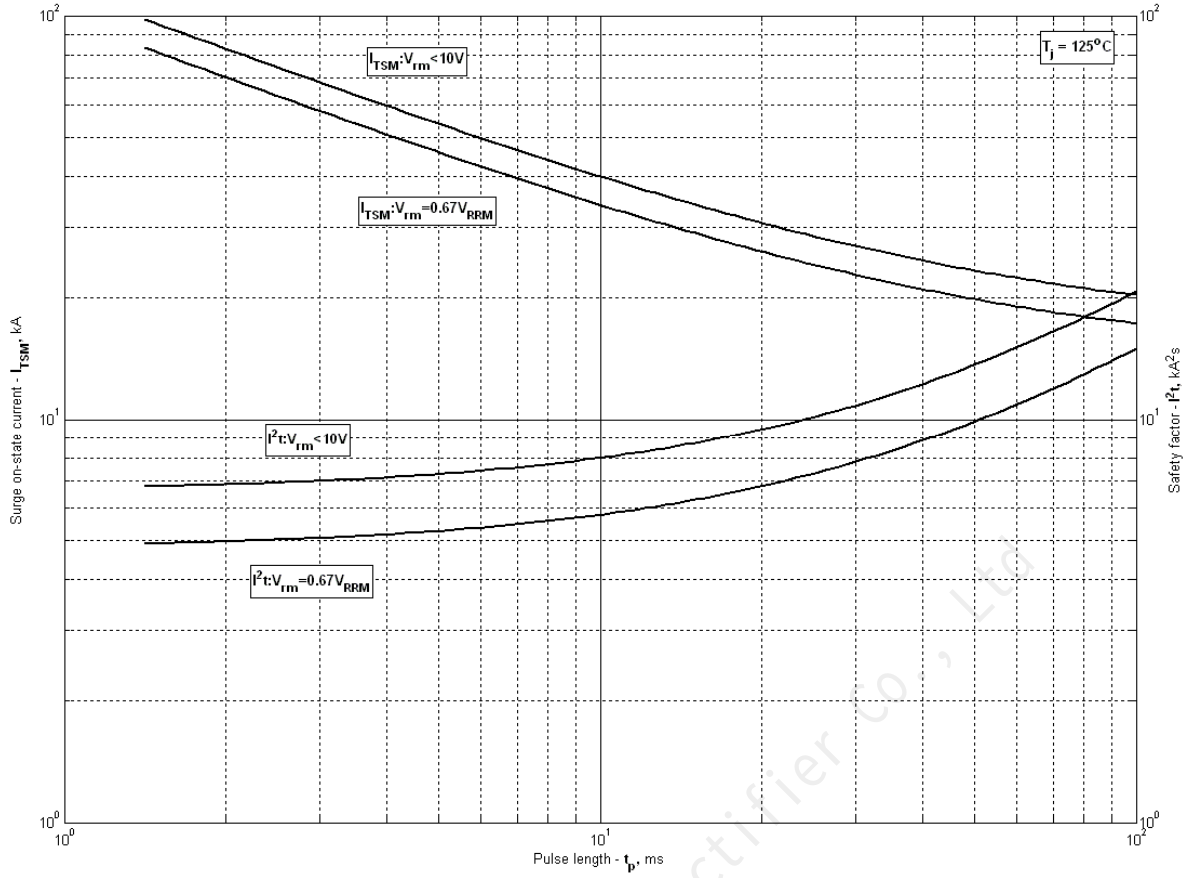



**Fig 13 – Maximum surge and $I^2t$ ratings**

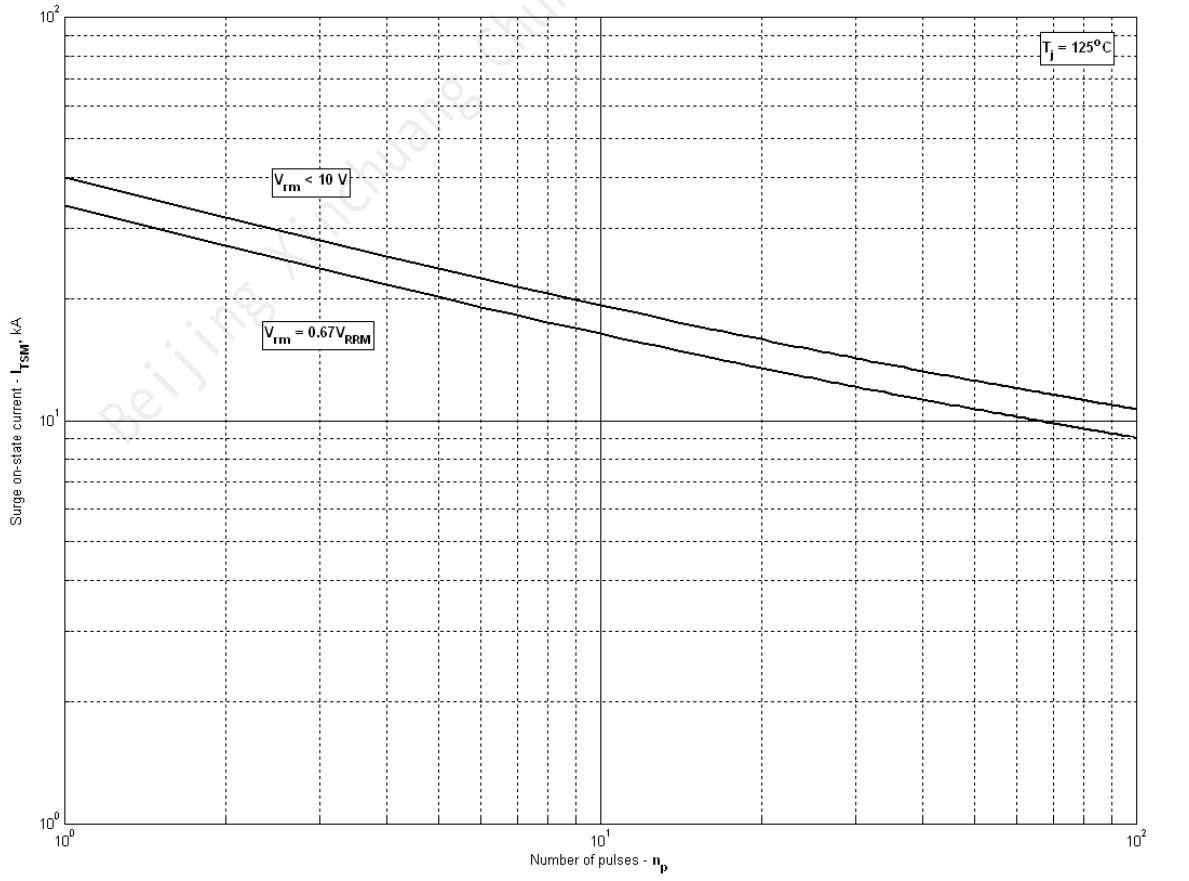



**Fig 14 – Maximum surge ratings**

