ChunZheng

High-end Power Semiconductor Manufacturer

KP2000A 4600V-5200V

Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current		I_{TAV}	2000 A	
Repetitive peak off-state voltage		V_{DRM}	4600 – 5200 V	
Repetitive peak reverse voltage		V_{RRM}		
Turn-off time		t_q	800 µs	
V_{DRM}, V_{RRM}, V	4600	4800	5000	5200
Voltage code	46	48	50	52
T_j, °C	– 60 – 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	2000	T_c= 85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	3140	T_c= 85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	42.0 48.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			45.0 52.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
I^2t	Safety factor	$A^2s{\cdot}10^3$	8820 11520	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
			8400 11220	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 µs; di_G/dt≥1 A/µs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	4600–5200	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	4700–5300	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

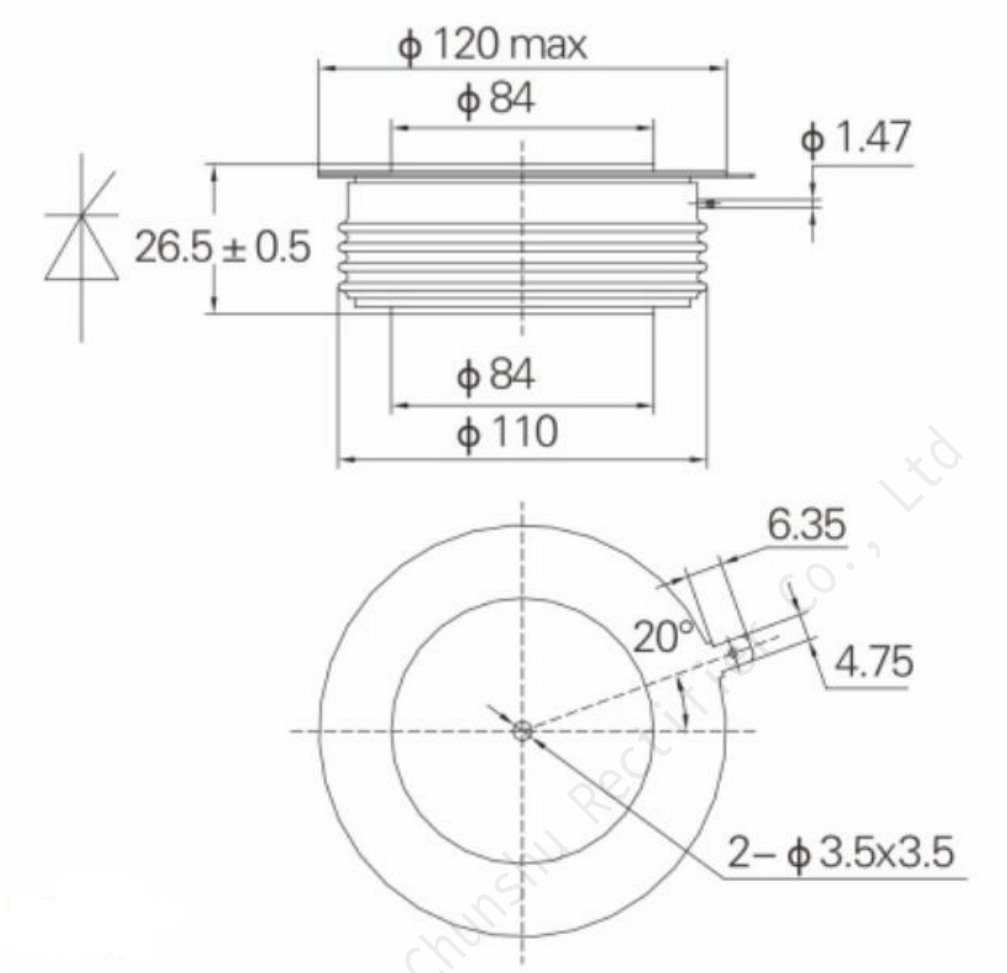
TRIGGERING				
I_{FGM}	Peak forward gate current	A	10	$T_j=T_{j\,max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j=T_{j\,max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	800	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60 – 125	
T_j	Operating junction temperature	°C	-60 – 125	
MECHANICAL				
F	Mounting force	kN	60.0 – 70.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	2.60	$T_j=25$ °C; $I_{TM}=6300$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	1.10	$T_j=T_{j\,max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	0.300		
I_L	Latching current, max	mA	1500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs	
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	200	$T_j=T_{j\,max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	1000	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.00	$T_j=25$ °C $T_j=T_{j\,max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	300 200	$T_j=25$ °C $T_j=T_{j\,max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\,max}$; $V_D=0.67\cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	15.00		
SWITCHING					
t_{gd}	Delay time	μs	4.00	$T_j=25$ °C; $V_D=0.4\cdot V_{DRM}$; $I_{TM}=2000$ A; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt\geq 1$ A/μs	
t_q	Turn-off time[2)], max	μs	800	$dv_D/dt=50$ V/μs; $T_j=T_{j\,max}$; $I_{TM}=2000$ A; $di_R/dt=-10$ A/μs; $V_R=100$ V; $V_D=0.67\ V_{DRM}$;	
Q_{rr}	Total recovered charge, max	μC	8000	$T_j=T_{j\,max}$; $I_{TM}=2000$ A; $di_R/dt=-5$ A/μs; $V_R=100$ V	
t_{rr}	Reverse recovery time, typ	μs	84		
I_{rrM}	Peak reverse recovery current, max	A	190		

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0065	Direct current	Double side cooled
R_{thjc-A}			0.0143		Anode side cooled
R_{thjc-K}			0.0117		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0015	Direct current	
MECHANICAL					
w	Weight, typ	g	1900		
D_s	Surface creepage distance	mm (inch)	36.50 (1.437)		
D_a	Air strike distance	mm (inch)	16.5 (0.650)		

OVERALL DIMENSIONS



KT90

All dimensions in millimeters

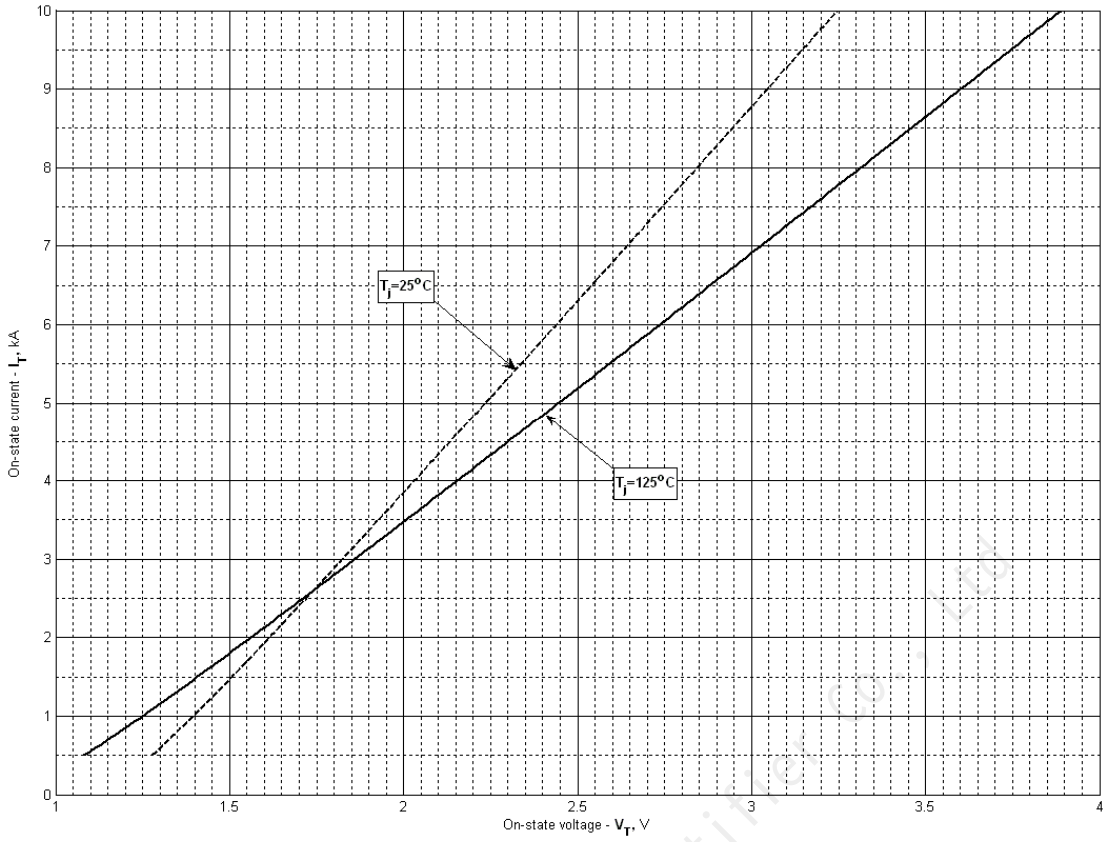


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	T_j = $T_{j\,max}$
A	1.067403	0.793378
B	0.171446	0.247535
C	-0.163288	-0.218083
D	0.270001	0.360605

On-state characteristic model (see Fig. 1)

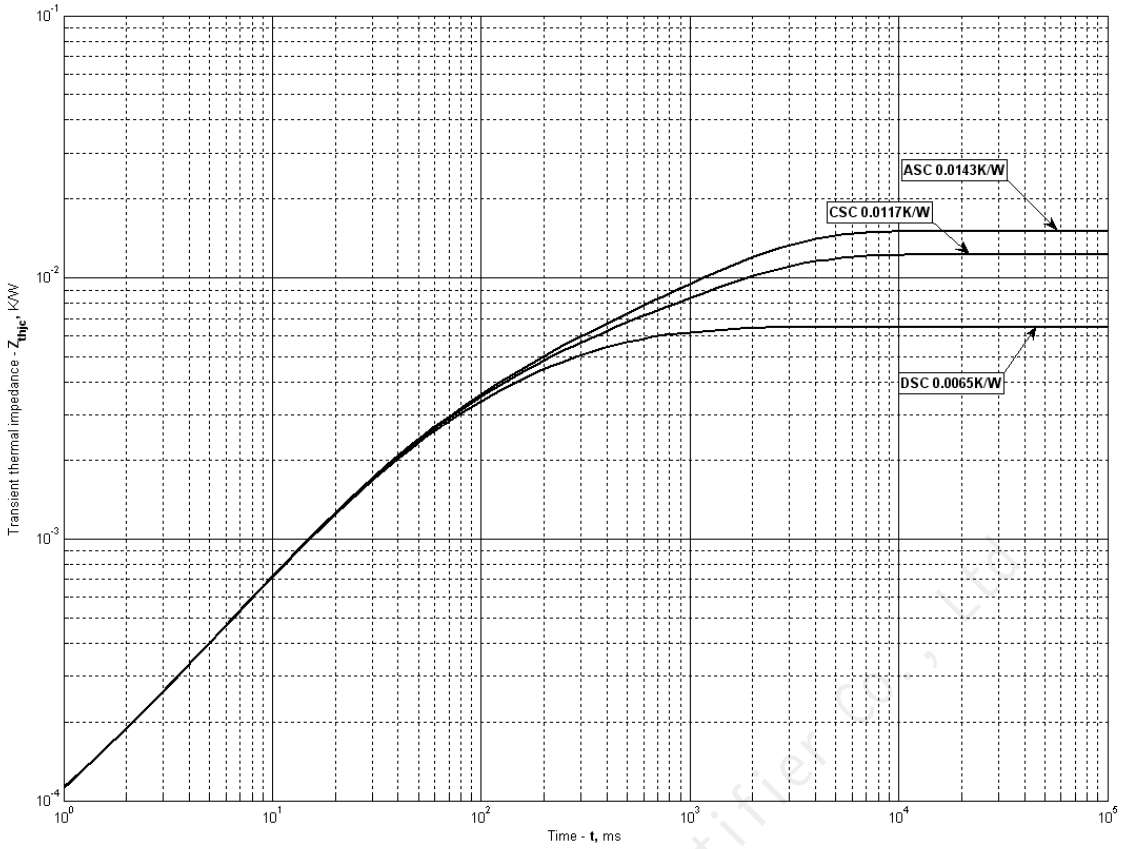


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

$\boldsymbol{\tau_i}$ = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.001031	0.003117	0.001895	0.0004176	2.061e-005	1.999e-005
$\boldsymbol{\tau_i}$, **s**	0.7345	0.209	0.05291	0.01652	0.0006764	0.0002168

DC Cathode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.001475	0.005797	0.002722	0.001822	0.0003923	3.824e-005
$\boldsymbol{\tau_i}$, **s**	0.8755	1.835	0.1997	0.05221	0.01594	0.0003499

DC Anode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.00848	0.001792	0.002597	0.00179	0.0003904	3.851e-005
$\boldsymbol{\tau_i}$, **s**	1.845	0.9581	0.2011	0.05234	0.01605	0.0003606

Transient thermal impedance junction to case $\mathbf{Z_{thjc}}$ model (see Fig. 2)

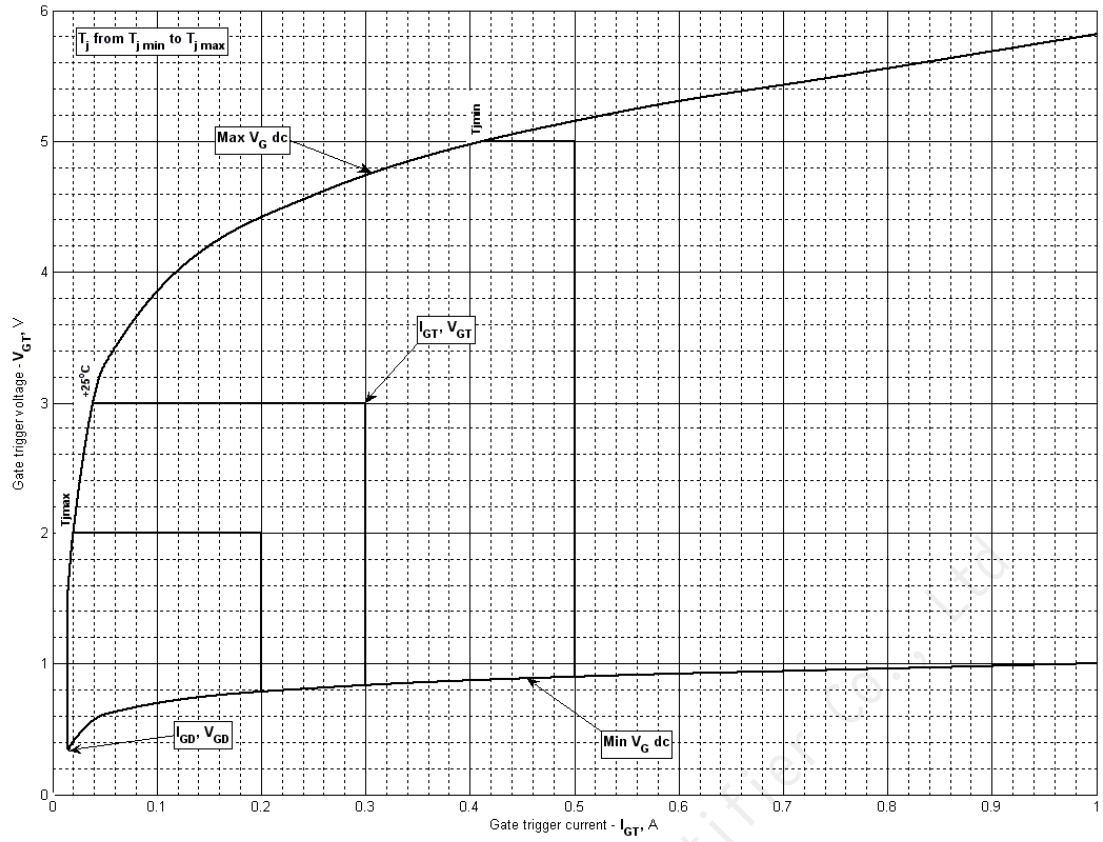


Fig 3 – Gate characteristics – Trigger limits

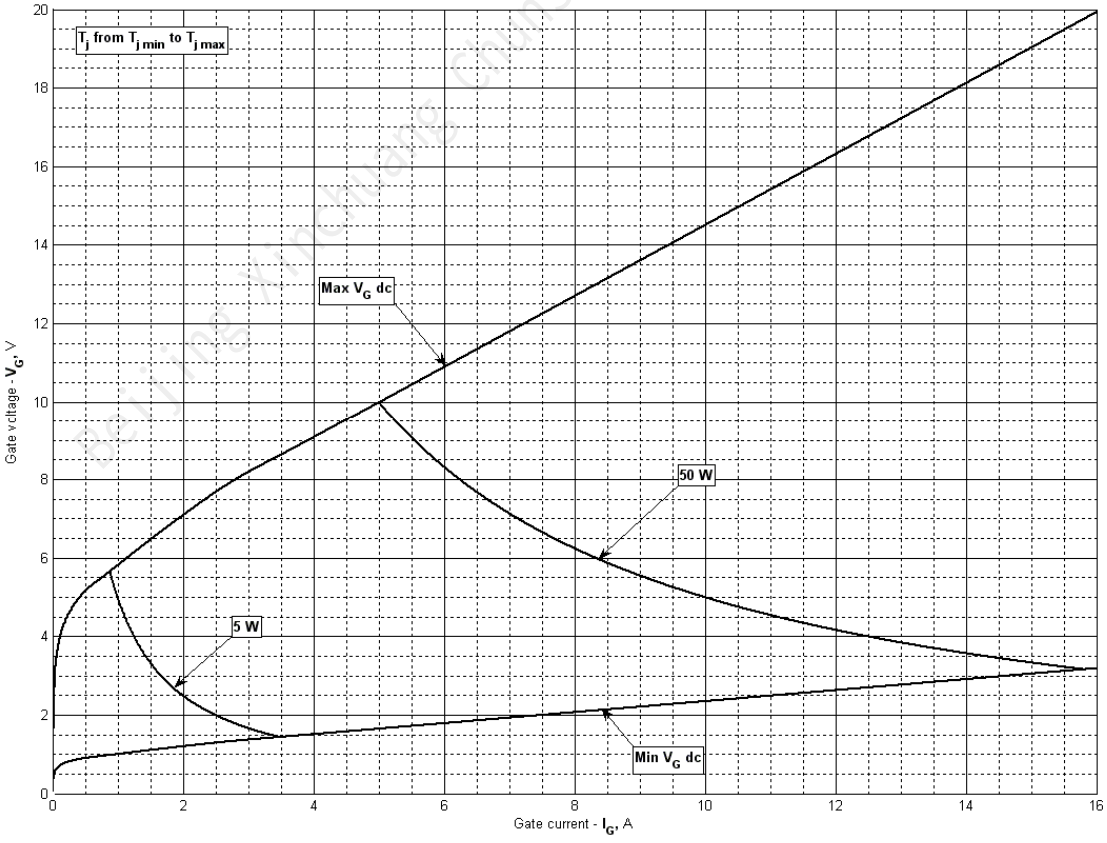


Fig 4 - Gate characteristics –Power curves

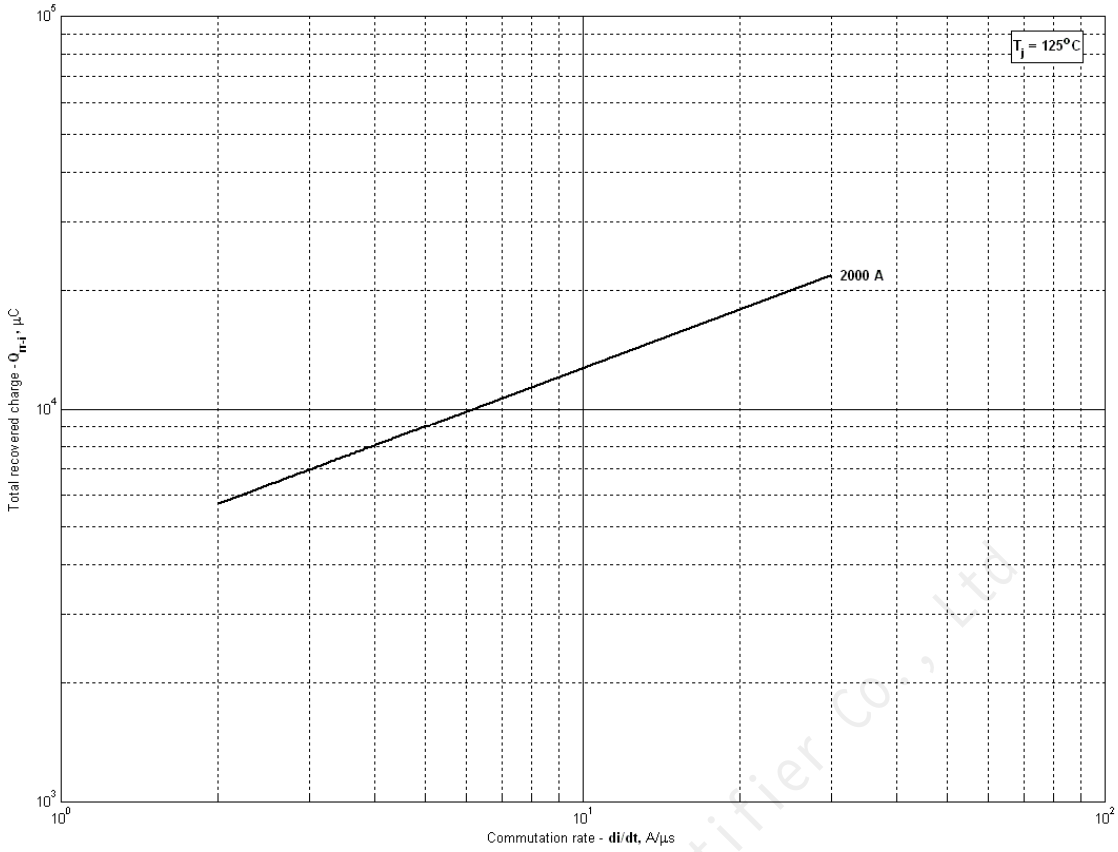


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

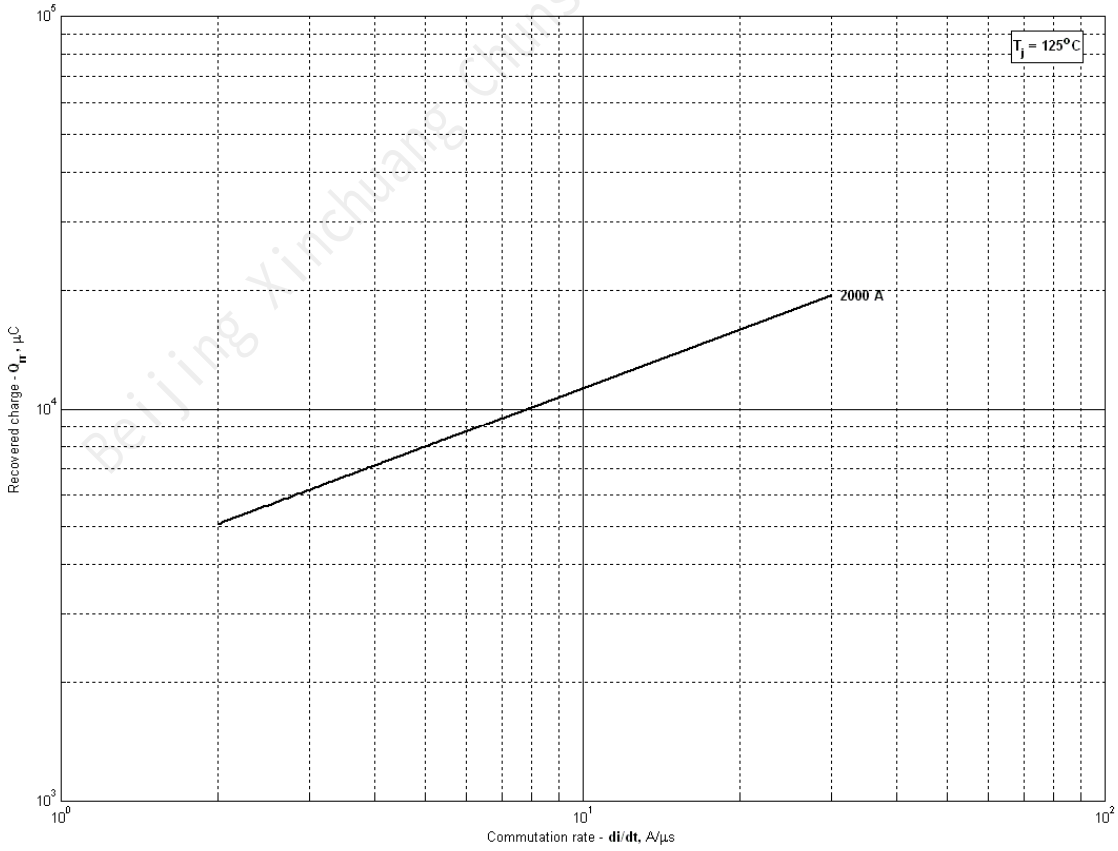


Fig 6 - Recovered charge, Q_{rr} (linear)

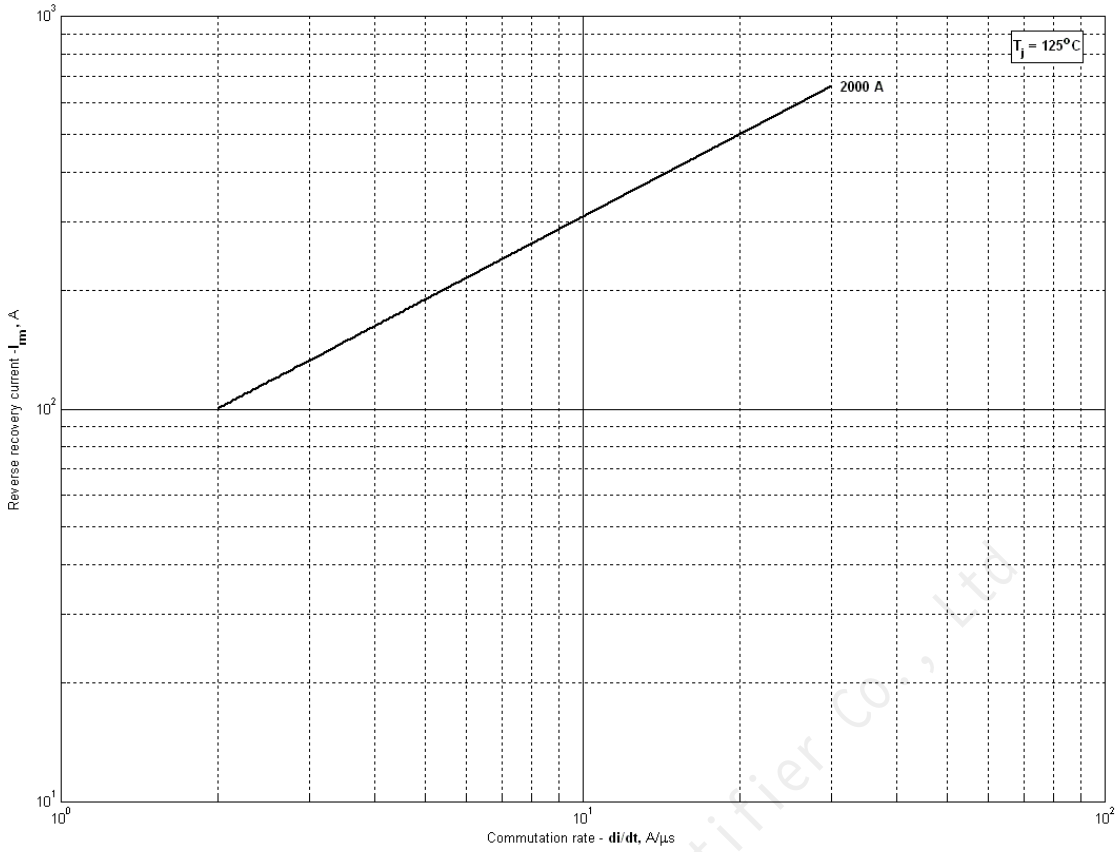


Fig 7 – Peak reverse recovery current, I_{rm}

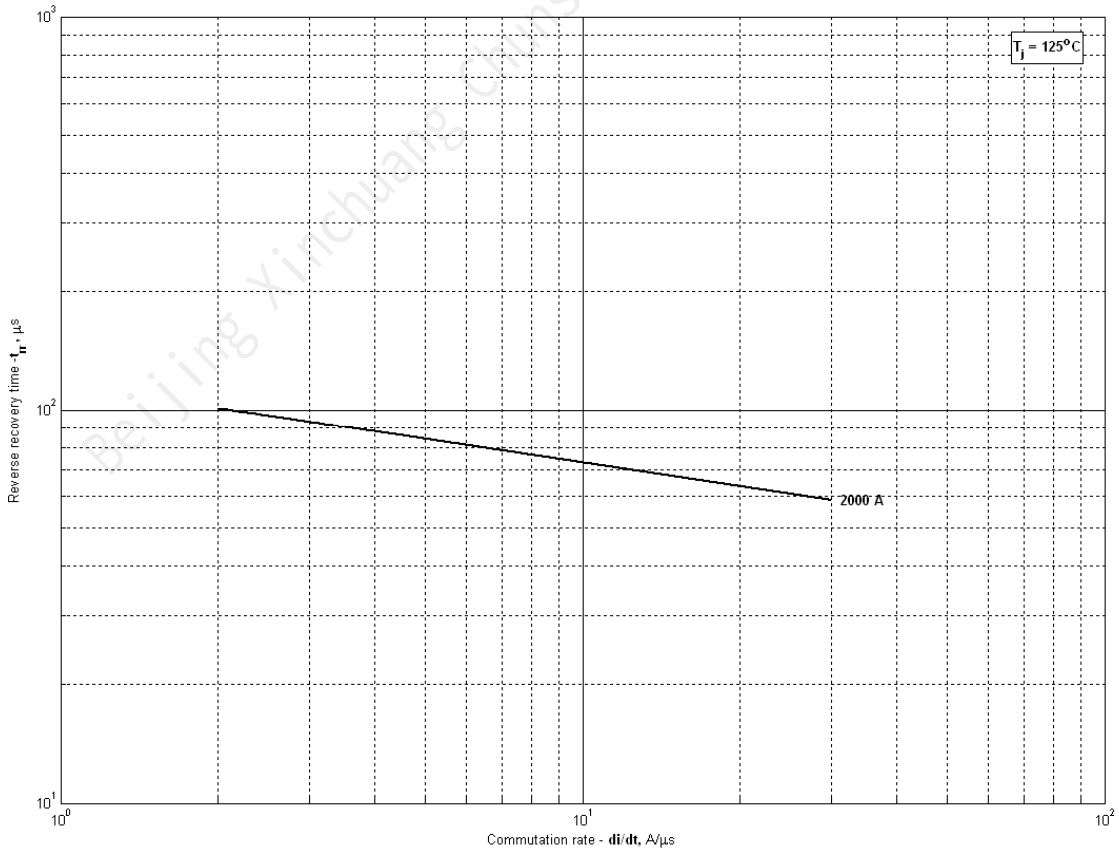


Fig 8 – Maximum recovery time, t_{rr} (linear)

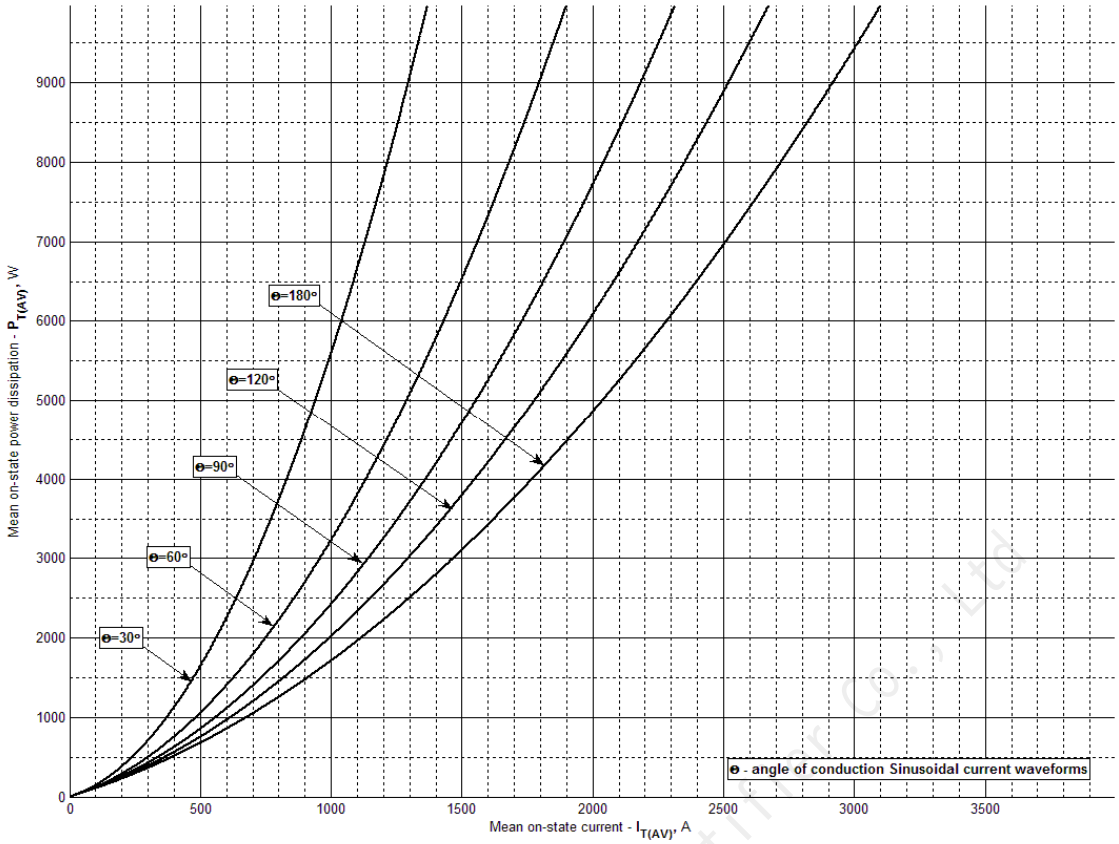


Fig 9 – On-state power loss (sinusoidal current waveforms)

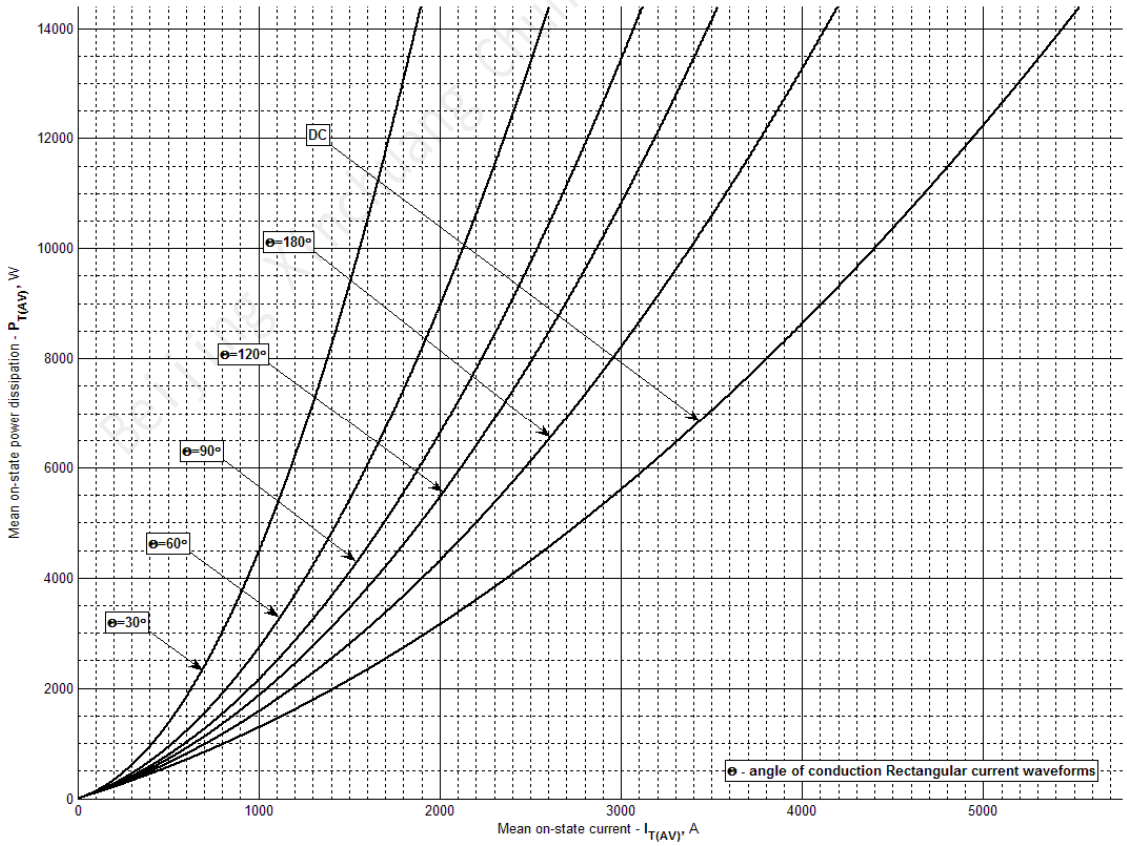


Fig 10 – On-state power loss (rectangular current waveforms)

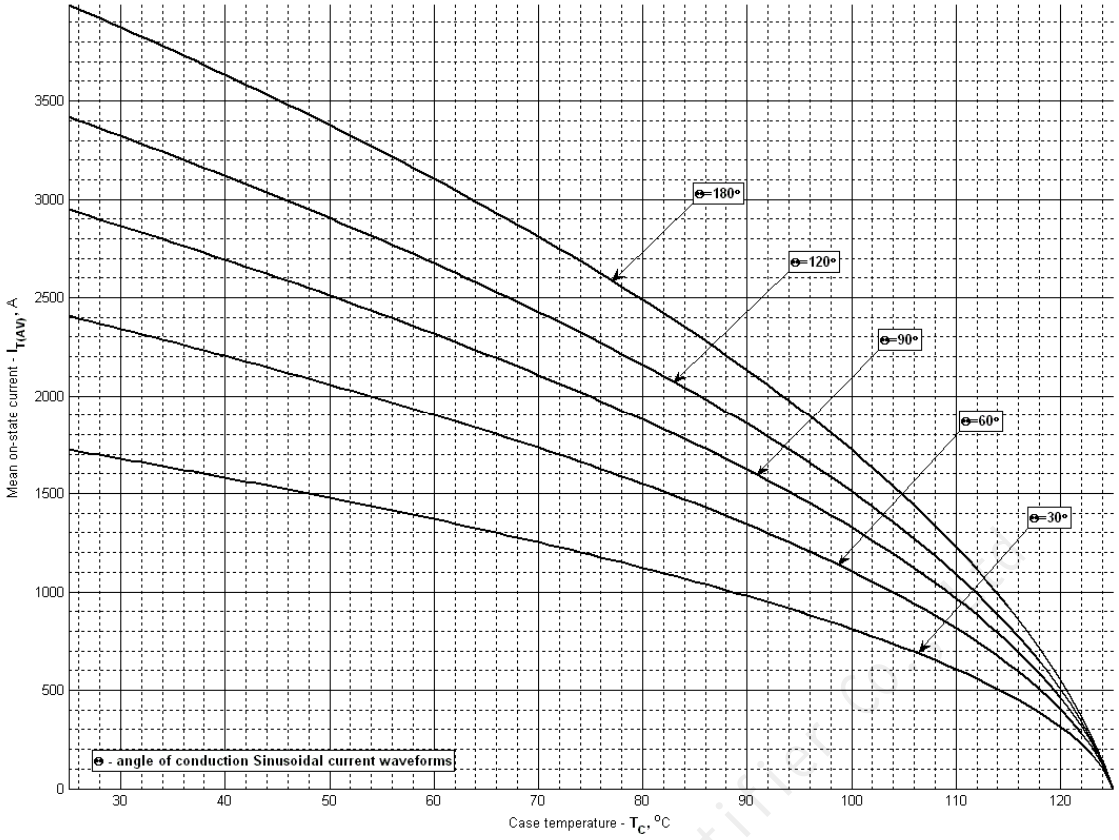


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

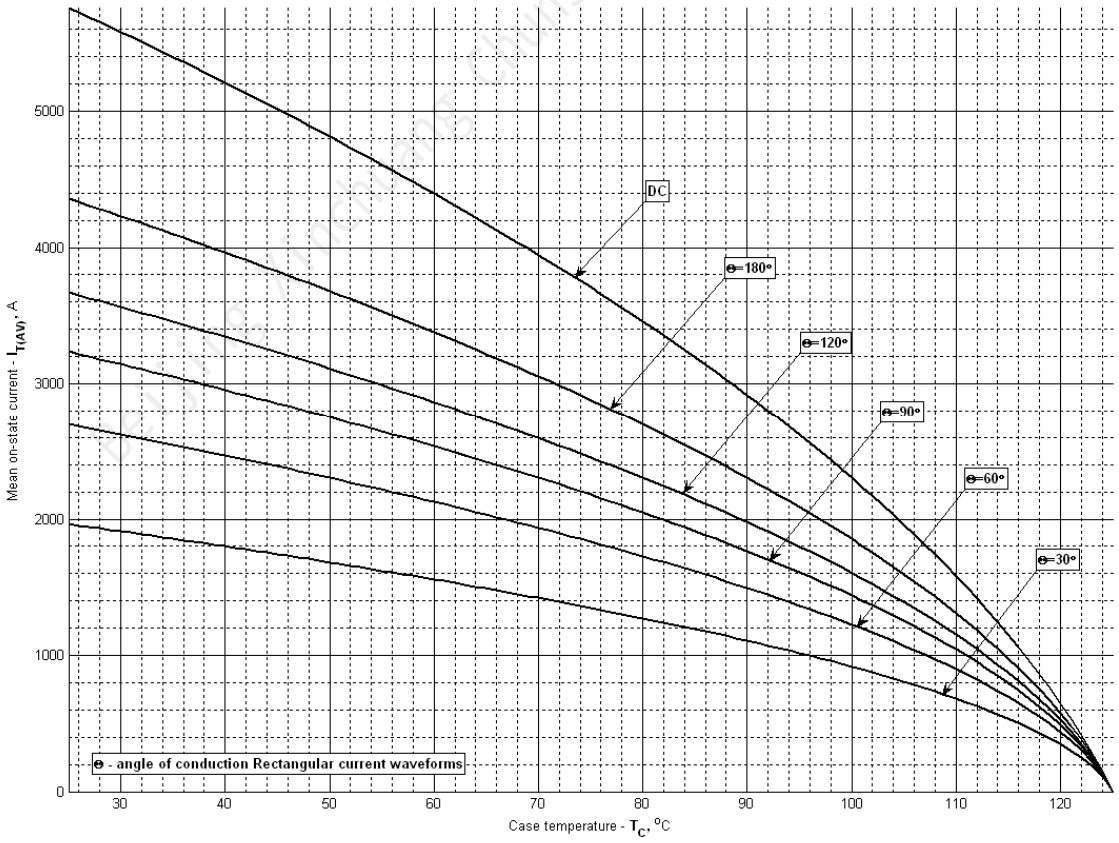


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

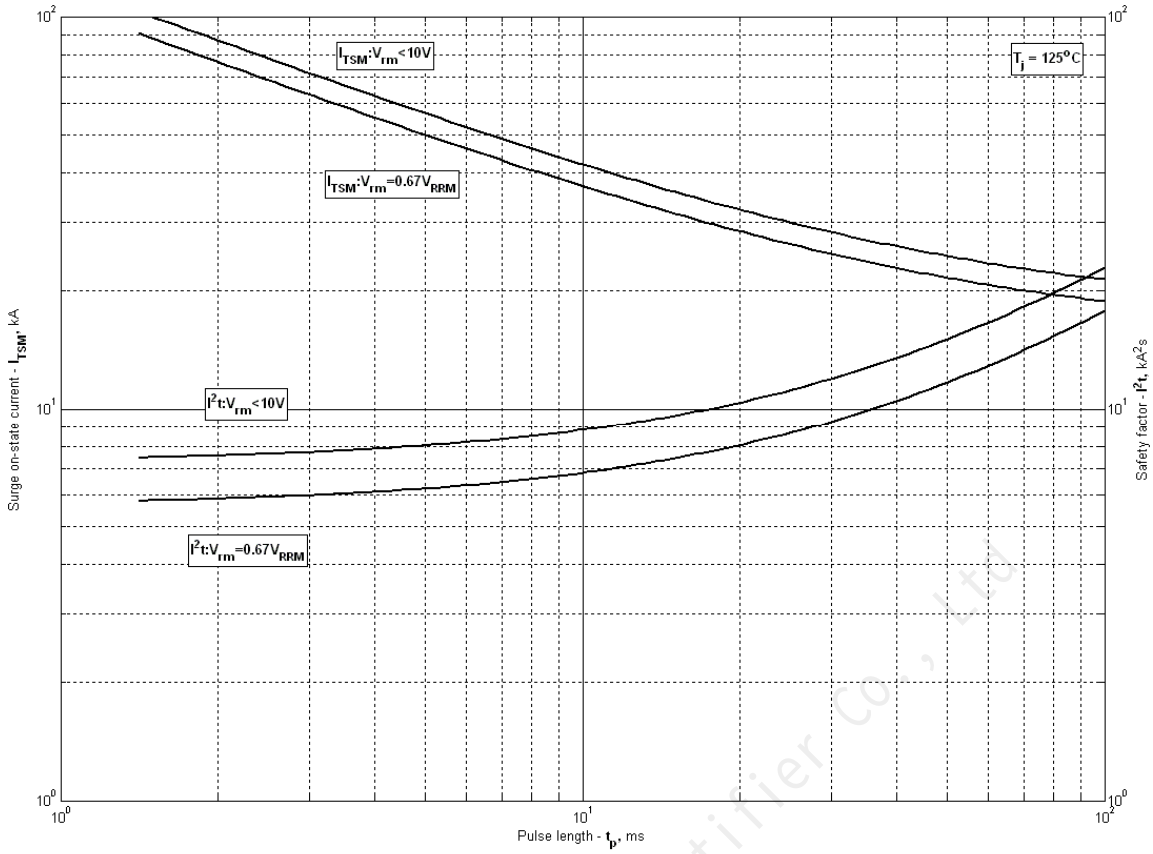


Fig 13 – Maximum surge and I^2t ratings

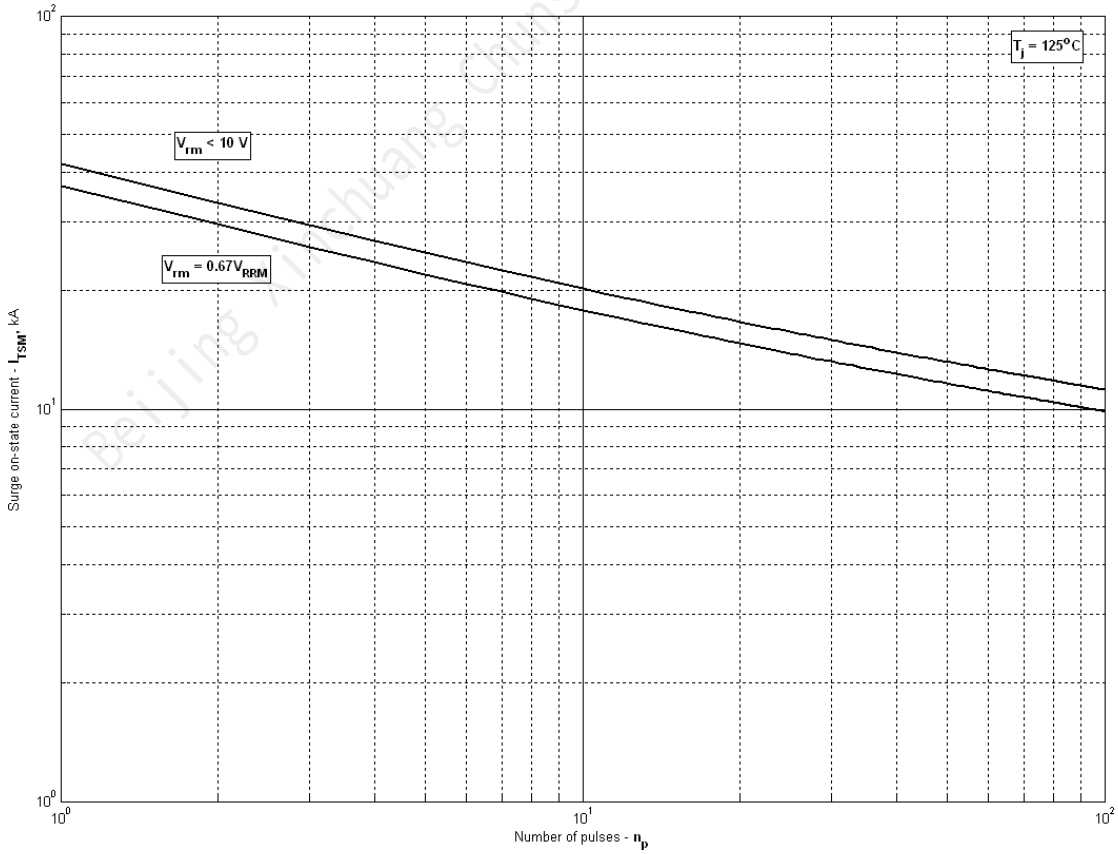


Fig 14 – Maximum surge ratings

