ChunZheng

High-end Power Semiconductor Manufacturer

KP4000A 2000V-2800V
Phase Control Thyristor

- High power cycling capability
- Low on-state and switching losses
- Designed for traction and industrial applications

Mean on-state current			I_{TAV}	4000 A	
Repetitive peak off-state voltage			V_{DRM}	2000 – 2800 V	
Repetitive peak reverse voltage			V_{RRM}		
Turn-off time			t_q	500 μs	
V_{DRM}, V_{RRM}, V	2000	2200	2400	2600	2800
Voltage code	20	22	24	26	28
T_j, °C	– 60 – 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	Values	Test conditions	
ON-STATE					
I_{TAV}	Mean on-state current	A	4000	T_c=85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TRMS}	RMS on-state current	A	6280	T_c= 85 °C, Double side cooled 180° half-sine wave; 50 Hz	
I_{TSM}	Surge on-state current	kA	75.0 86.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			79.0 91.0	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
I^2t	Safety factor	$A^2s{\cdot}10^3$	28125 36980	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 50 Hz (t_p=10 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
			25900 34365	T_j=$T_{j\,max}$ T_j=25 °C	180° half-sine wave; 60 Hz (t_p=8.3 ms); single pulse; V_D=V_R=0 V; Gate pulse: I_G=2 A; t_{GP}=50 μs; di_G/dt≥1 A/μs
BLOCKING					
V_{DRM}, V_{RRM}	Repetitive peak off-state and Repetitive peak reverse voltages	V	2000–2800	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz; Gate open	
V_{DSM}, V_{RSM}	Non-repetitive peak off-state and Non-repetitive peak reverse voltages	V	2100–2900	$T_{j\,min}$< T_j <$T_{j\,max}$; 180° half-sine wave; 50 Hz;single pulse; Gate open	
V_D, V_R	Direct off-state and Direct reverse voltages	V	0.75·V_{DRM} 0.75·V_{RRM}	T_j=$T_{j\,max}$; Gate open	

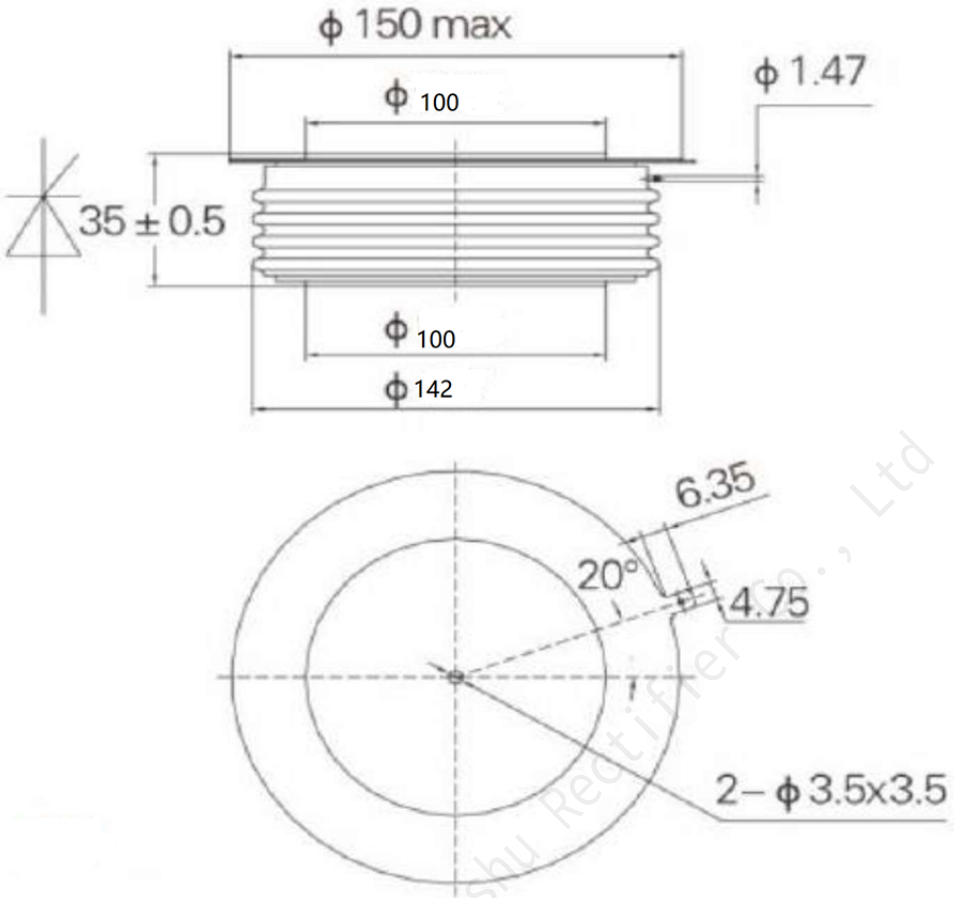
TRIGGERING				
I_{FGM}	Peak forward gate current	A	12	$T_j=T_{j\ max}$
V_{RGM}	Peak reverse gate voltage	V	5	
P_G	Gate power dissipation	W	5	$T_j=T_{j\ max}$ for DC gate current
SWITCHING				
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current non-repetitive (f=1 Hz)	A/μs	1000	$T_j=T_{j\ max}$; $V_D=0.67 \cdot V_{DRM}$; $I_{TM}=2\ I_{TAV}$; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 1$ A/μs
THERMAL				
T_{stg}	Storage temperature	°C	-60 – 125	
T_j	Operating junction temperature	°C	-60 – 125	
MECHANICAL				
F	Mounting force	kN	70.0 – 90.0	
a	Acceleration	m/s^2	50 100	Device unclamped Device clamped

CHARACTERISTICS

Symbols and parameters		Units	Values	Conditions	
ON-STATE					
V_{TM}	Peak on-state voltage, max	V	1.55	$T_j=25$ °C; $I_{TM}=6300$ A	
$V_{T(TO)}$	On-state threshold voltage, max	V	0.95	$T_j=T_{j\ max}$; $0.5\ \pi\ I_{TAV} < I_T < 1.5\ \pi\ I_{TAV}$	
r_T	On-state slope resistance, max	mΩ	0.080		
I_L	Latching current, max	mA	1500	$T_j=25$ °C; $V_D=12$ V; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 1$ A/μs	
I_H	Holding current, max	mA	300	$T_j=25$ °C; $V_D=12$ V; Gate open	
BLOCKING					
I_{DRM}, I_{RRM}	Repetitive peak off-state and Repetitive peak reverse currents, max	mA	300	$T_j=T_{j\ max}$; $V_D=V_{DRM}$; $V_R=V_{RRM}$	
$(dv_D/dt)_{crit}$	Critical rate of rise of off-state voltage[1)], min	V/μs	1000	$T_j=T_{j\ max}$; $V_D=0.67 \cdot V_{DRM}$; Gate open	
TRIGGERING					
V_{GT}	Gate trigger direct voltage, max	V	3.00 2.00	$T_j=25$ °C $T_j=T_{j\ max}$	$V_D=12$ V; $I_D=3$ A; Direct gate current
I_{GT}	Gate trigger direct current, max	mA	300 200	$T_j=25$ °C $T_j=T_{j\ max}$	
V_{GD}	Gate non-trigger direct voltage, min	V	0.35	$T_j=T_{j\ max}$; $V_D=0.67 \cdot V_{DRM}$; Direct gate current	
I_{GD}	Gate non-trigger direct current, min	mA	15.00		
SWITCHING					
t_{gd}	Delay time	μs	2.50	$T_j=25$ °C; $V_D=0.4 \cdot V_{DRM}$; $I_{TM}=2000$ A; Gate pulse: $I_G=2$ A; $t_{GP}=50$ μs; $di_G/dt \geq 1$ A/μs	
t_q	Turn-off time[2)], max	μs	500	$dv_D/dt=50$ V/μs; $T_j=T_{j\ max}$; $I_{TM}=2000$ A; $di_R/dt=-10$ A/μs; $V_R=100$ V; $V_D=0.67\ V_{DRM}$;	

THERMAL					
R_{thjc}	Thermal resistance, junction to case, max	°C/W	0.0057	Direct current	Double side cooled
R_{thjc-A}			0.0125		Anode side cooled
R_{thjc-K}			0.0103		Cathode side cooled
R_{thck}	Thermal resistance, case to heatsink, max	°C/W	0.0010	Direct current	
MECHANICAL					
w	Weight, typ	g	2700		
D_s	Surface creepage distance	mm (inch)	62.09 (2.444)		
D_a	Air strike distance	mm (inch)	23.40 (0.921)		

OVERALL DIMENSIONS



KT110DT

All dimensions in millimeters

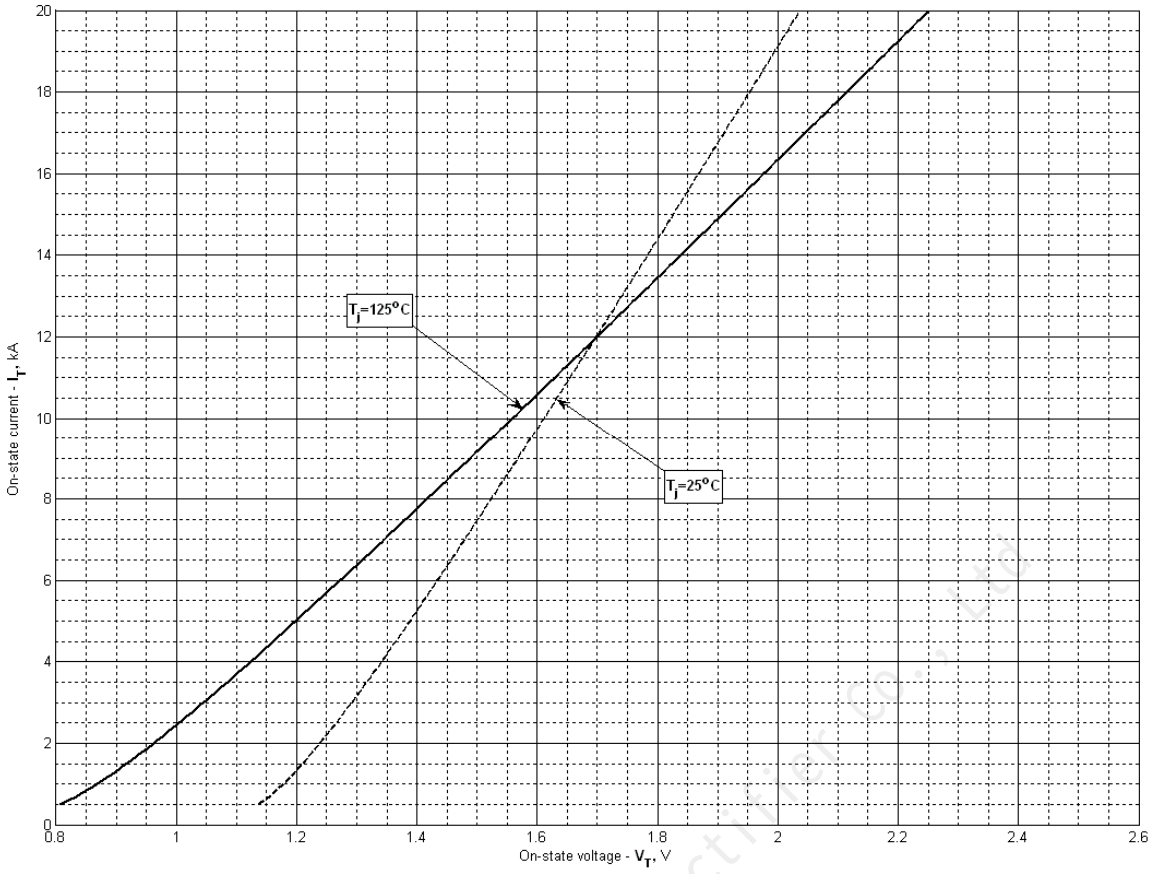


Fig 1 – On-state characteristics of Limit device

Analytical function for On-state characteristic:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

	Coefficients for max curves	
	T_j = 25°C	$T_j = T_{j\,max}$
A	1.142428	0.808713
B	0.048143	0.076708
C	0.144998	0.193655
D	-0.113913	-0.152139

On-state characteristic model (see Fig. 1)

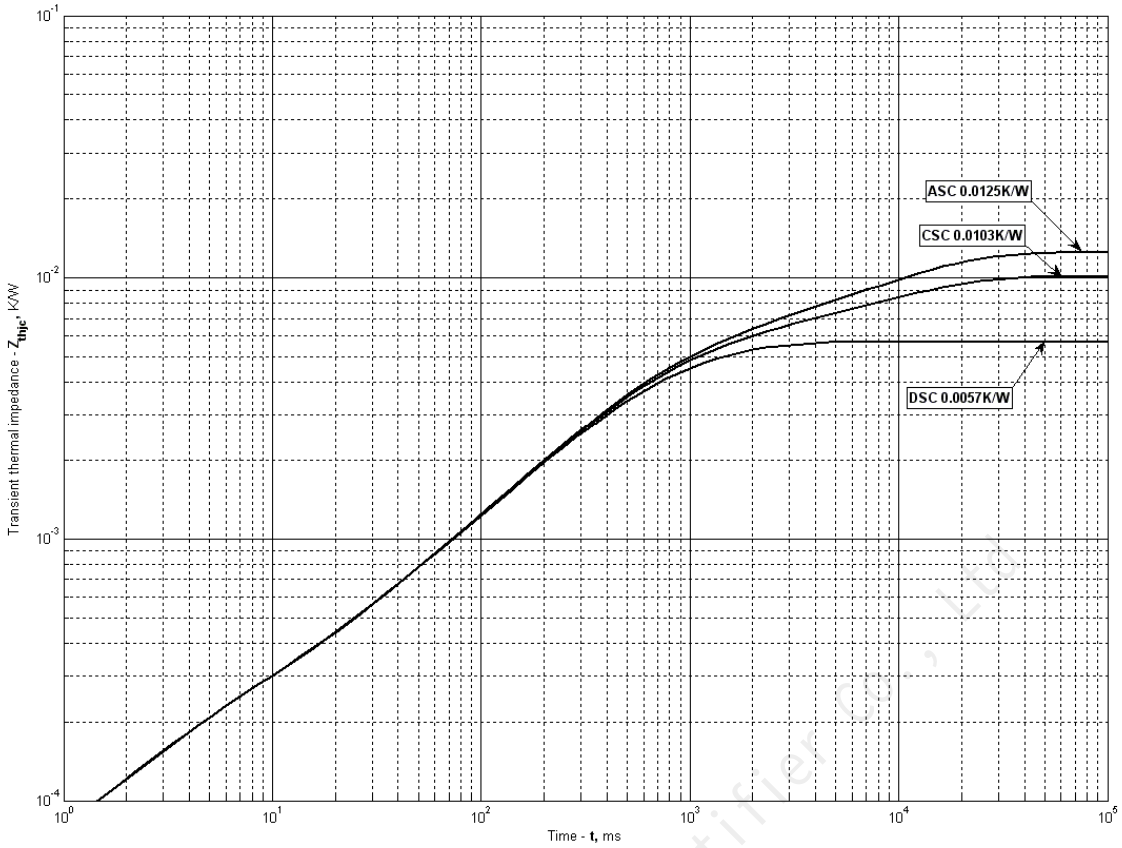


Fig 2 – Transient thermal impedance

Analytical function for Transient thermal impedance junction to case Z_{thjc} for DC:

$$Z_{thjc} = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

Where ***i*** = 1 to ***n***, ***n*** is the number of terms in the series.

t = Duration of heating pulse in seconds.

$\mathbf{Z_{thjc}}$ = Thermal resistance at time t.

$\mathbf{R_i}$ = Amplitude of p_{th} term.

τ_i = Time constatnt of r_{th} term.

DC Double side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.002457	-0.003548	0.002909	0.0002069	3.51e-005	0.00364
τ_i, **s**	1.062	0.005022	0.3787	0.0257	0.0003732	0.004916

DC Cathode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.004458	0.002601	0.002763	0.0001806	0.0001224	3.094e-005
τ_i, **s**	1.06	1.100	0.3794	0.0291	0.003057	0.0003374

DC Anode side cooled

i	1	2	3	4	5	6
$\mathbf{R_i}$, **K/W**	0.006812	0.002637	0.002729	0.0001806	0.000122	3.069e-005
τ_i, **s**	1.06	1.131	0.3835	0.02886	0.003033	0.0003349

Transient thermal impedance junction to case Z_{thjc} model (see Fig. 2)

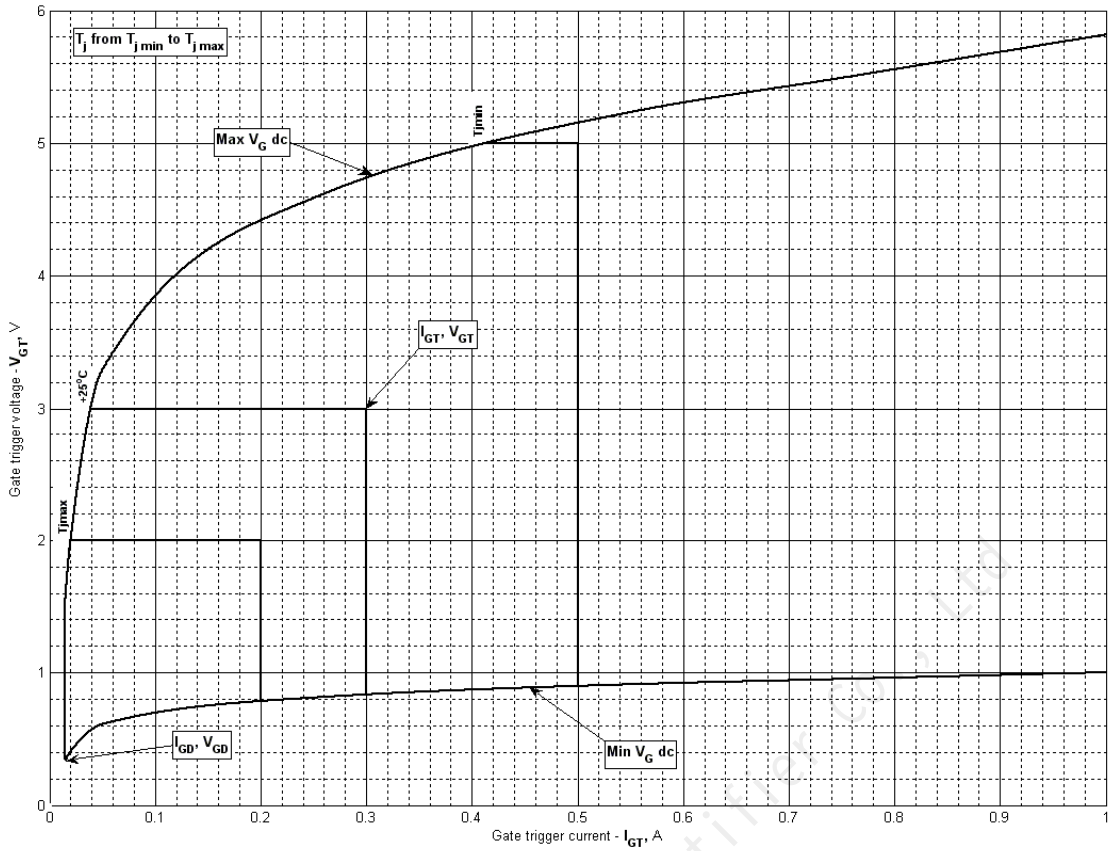


Fig 3 – Gate characteristics – Trigger limits

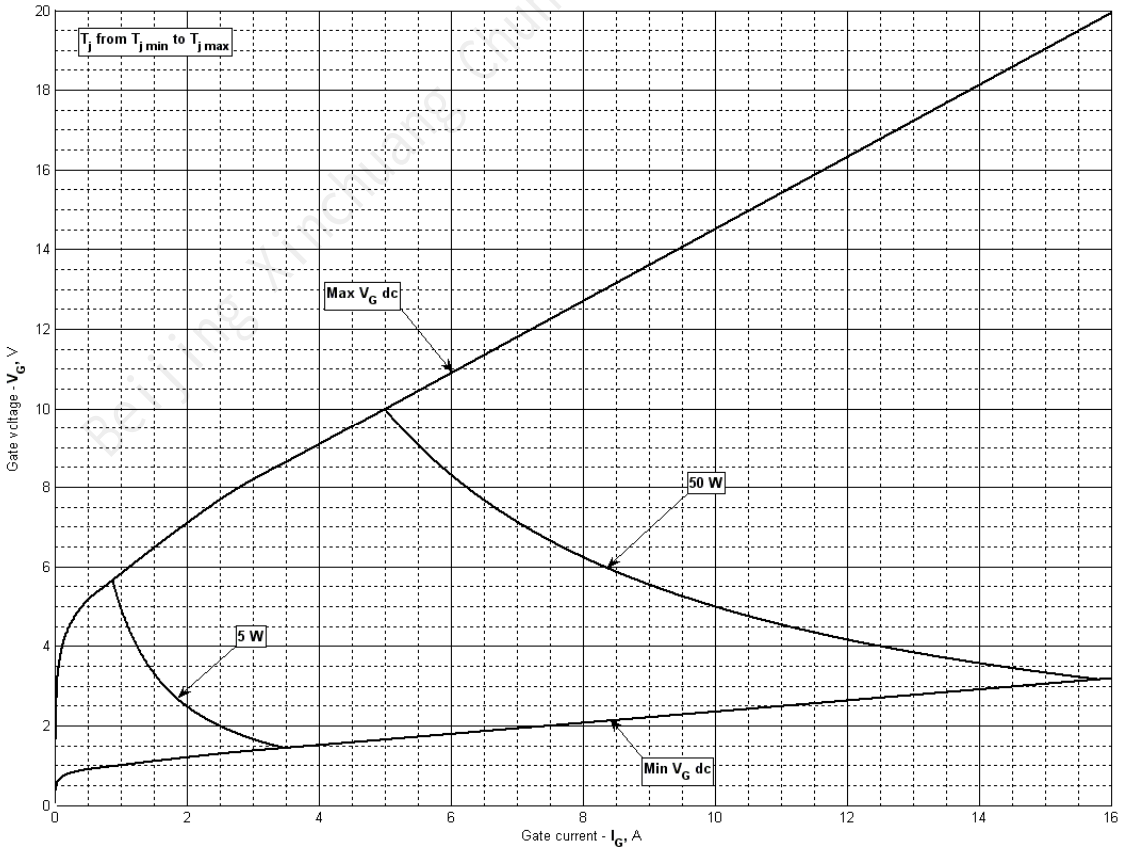


Fig 4 - Gate characteristics –Power curves

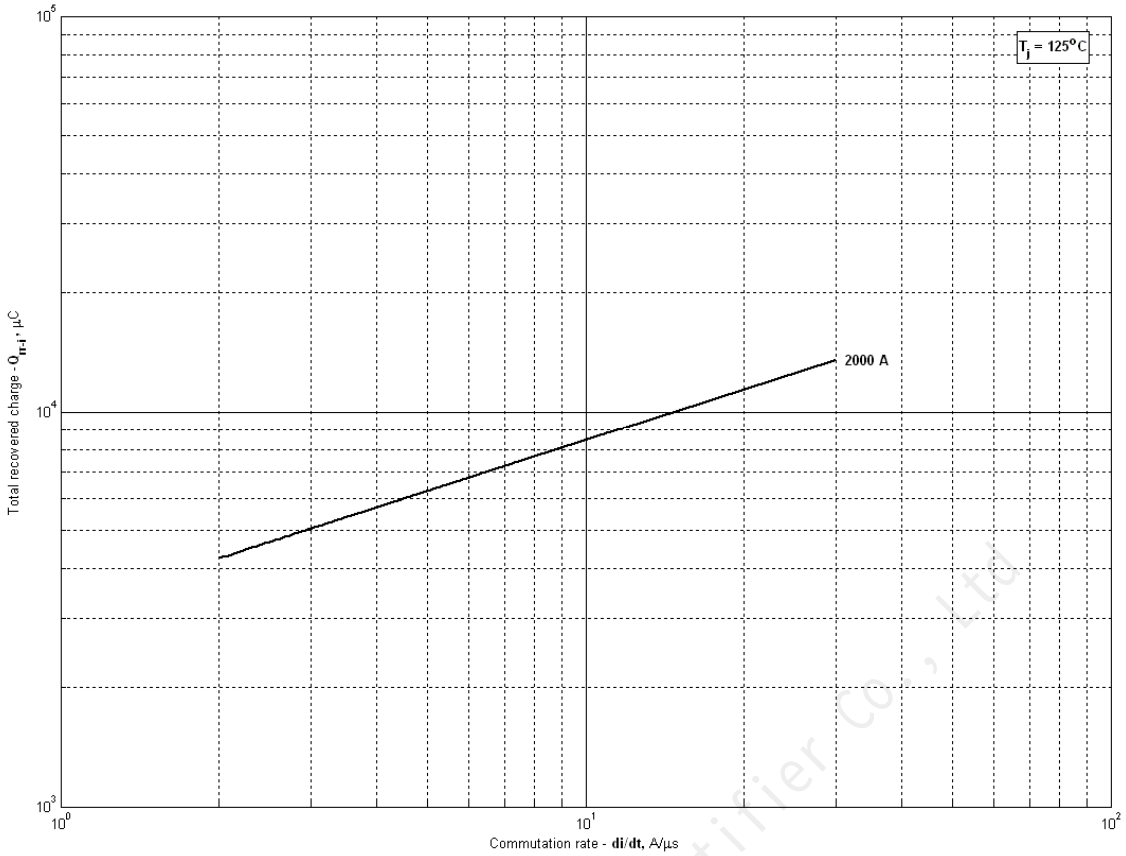


Fig 5 – Total recovered charge, Q_{rr-i} (integral)

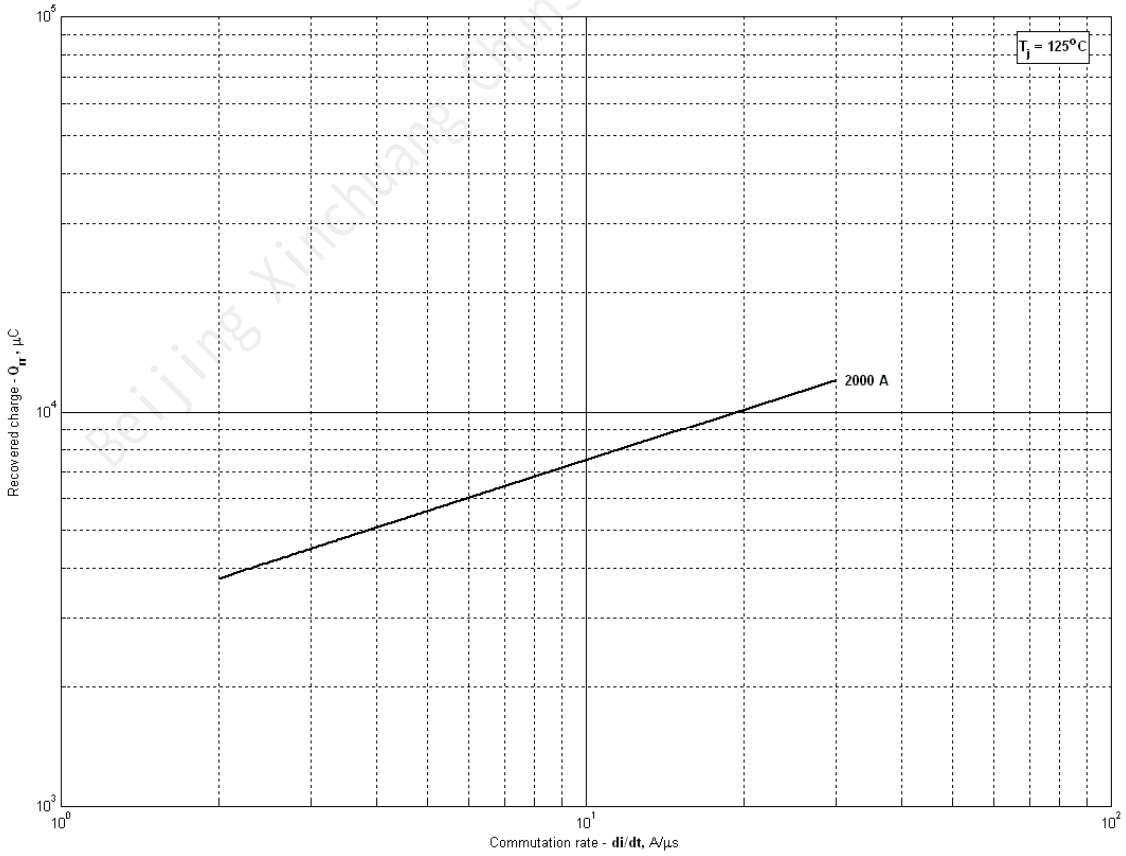


Fig 6 - Recovered charge, Q_{rr} (linear)

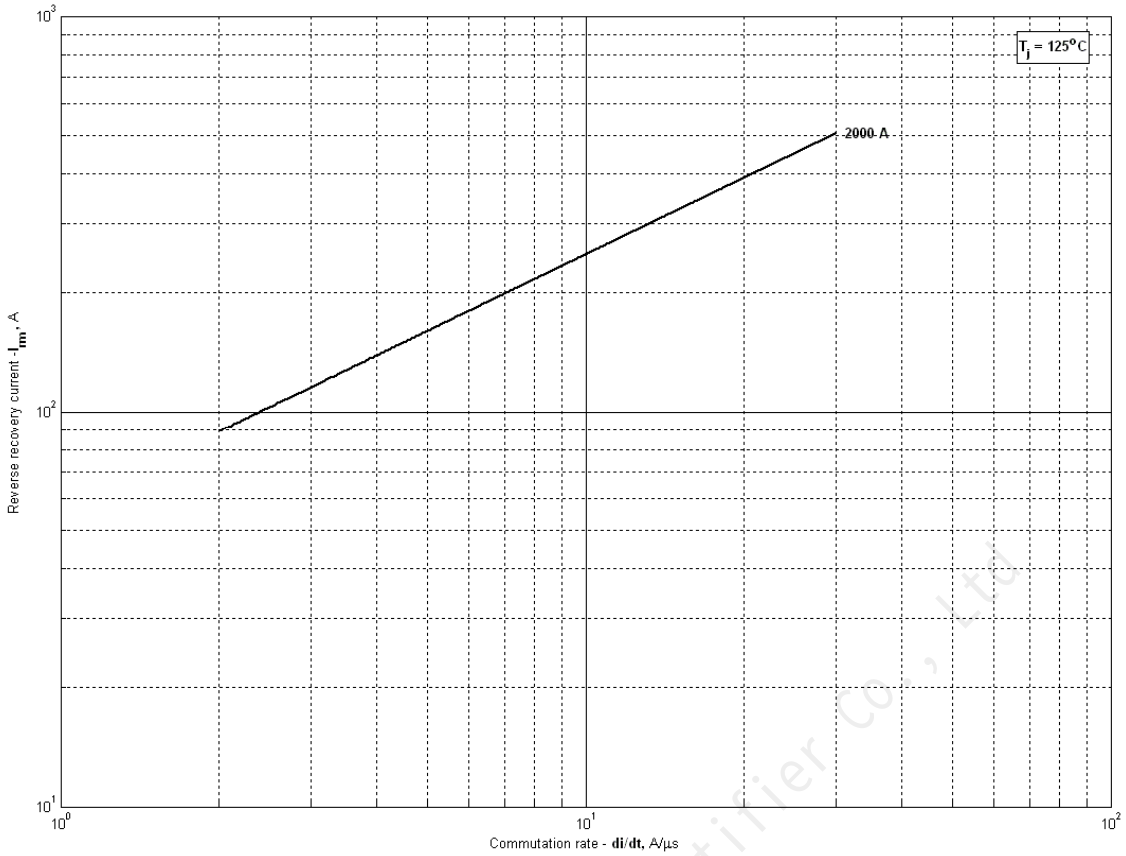


Fig 7 – Peak reverse recovery current, I_{rm}

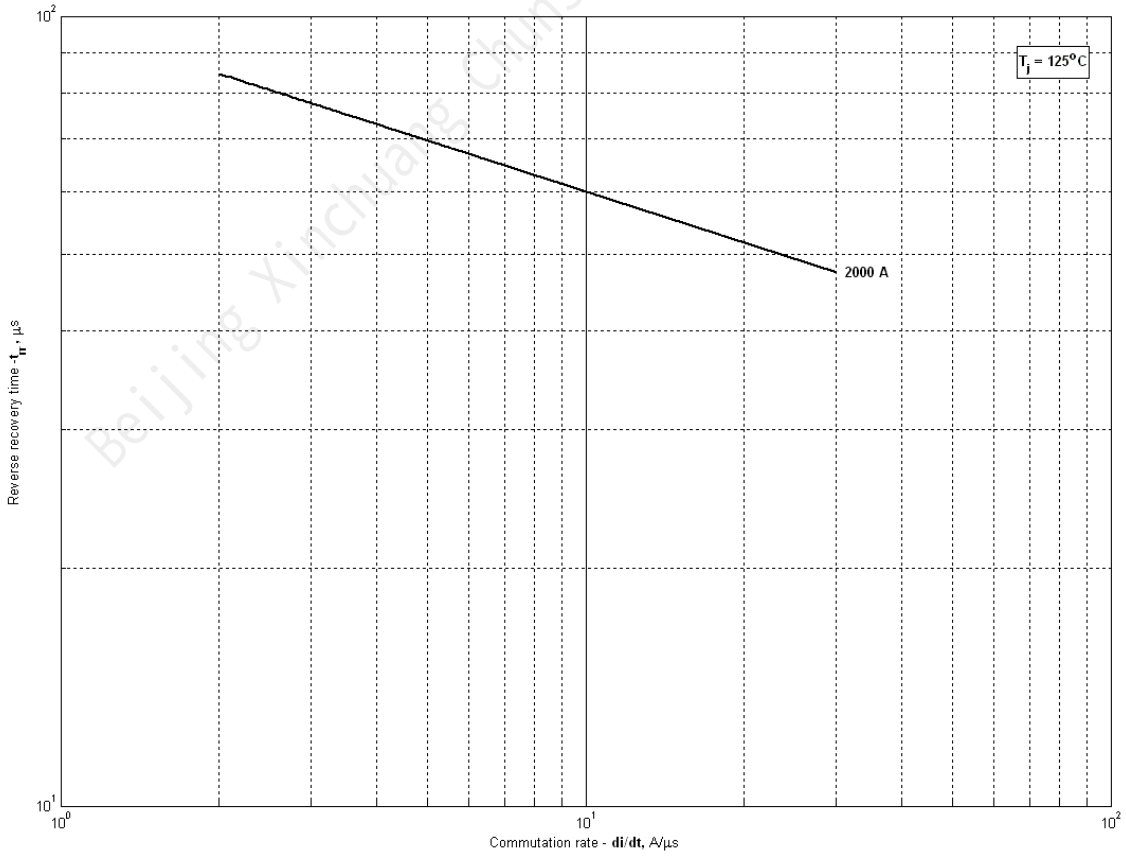


Fig 8 – Maximum recovery time, t_{rr} (linear)

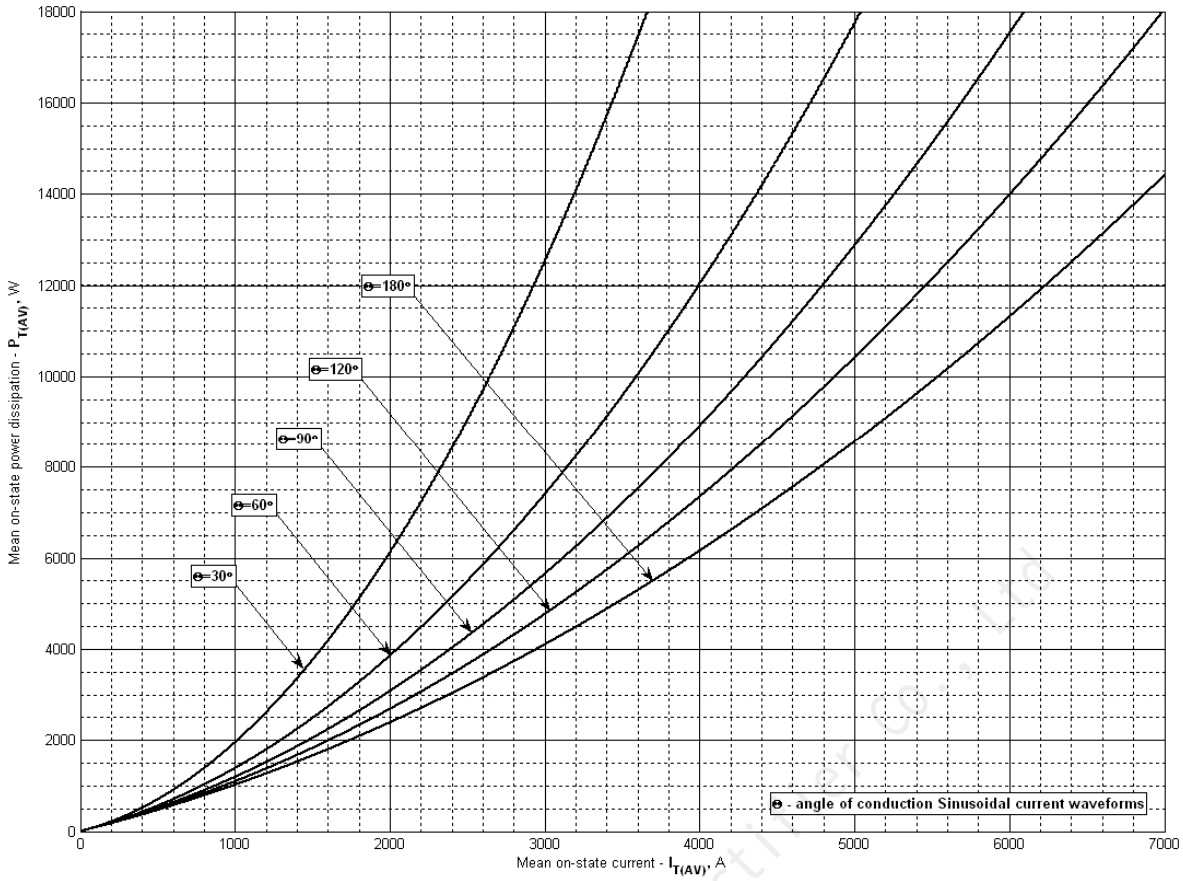


Fig 9 – On-state power loss (sinusoidal current waveforms)

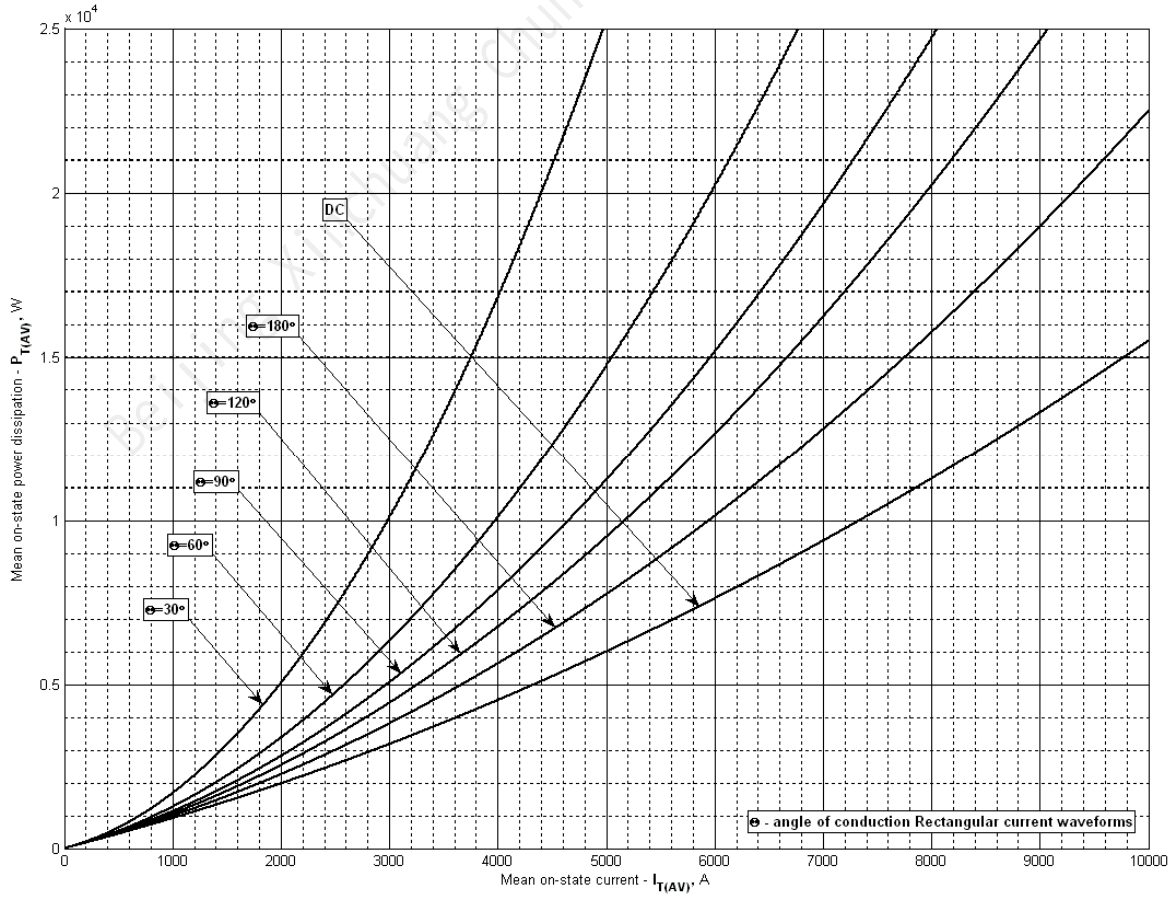


Fig 10 – On-state power loss (rectangular current waveforms)

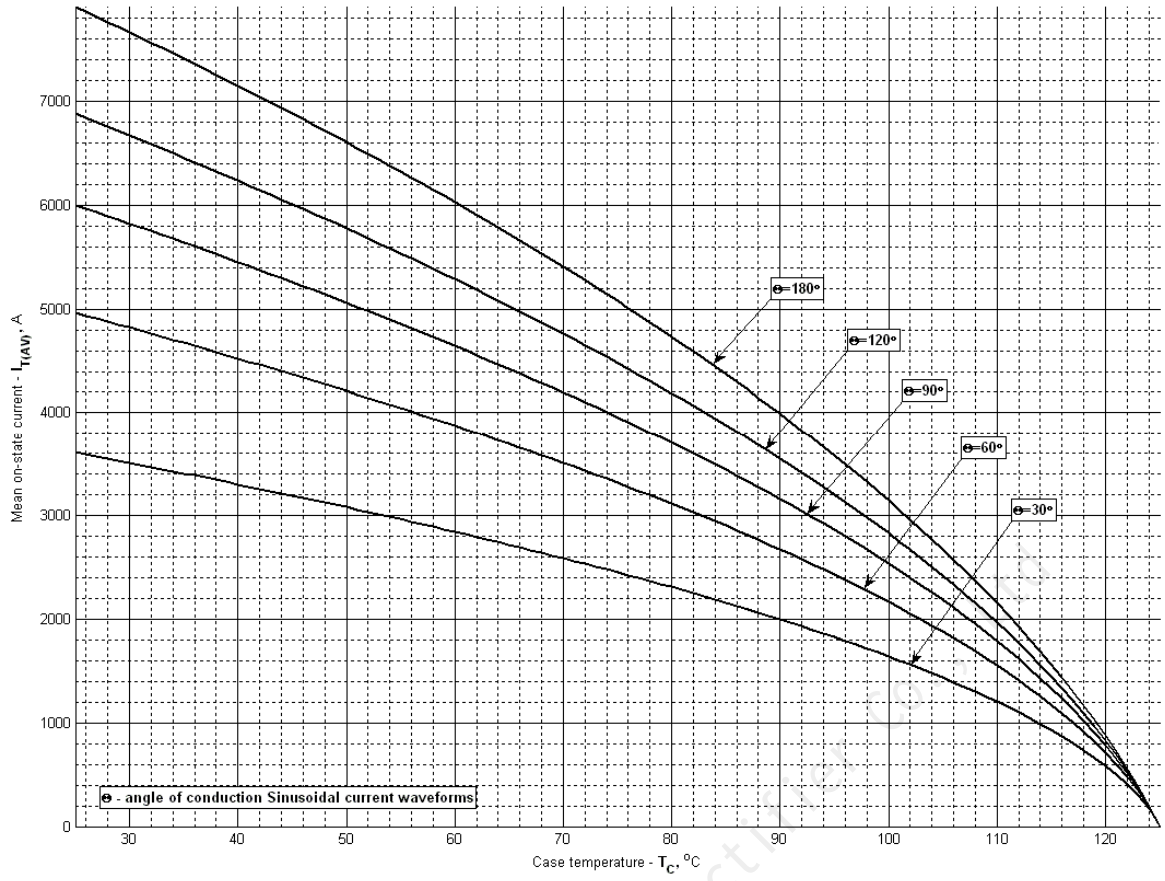


Fig 11 – Maximum case temperature DSC (sinusoidal current waveforms)

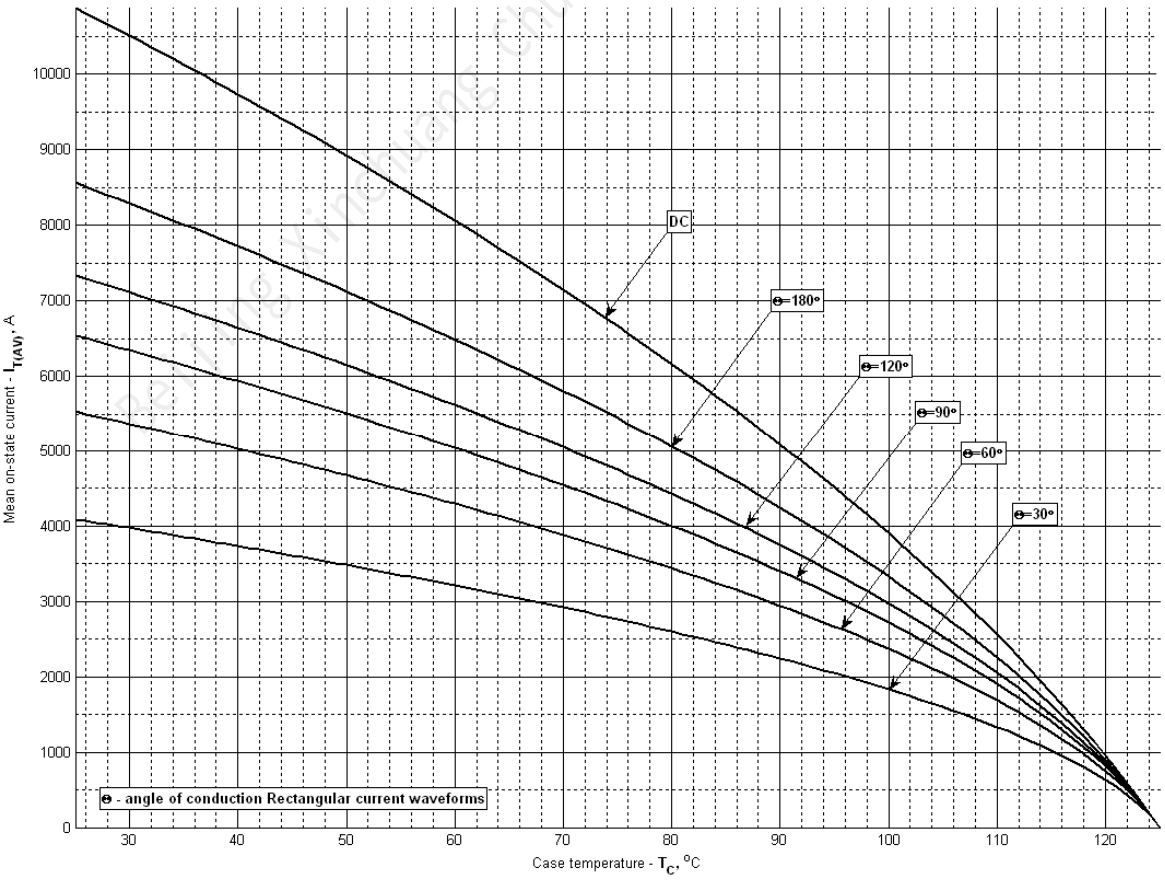


Fig 12 – Maximum case temperature DSC (rectangular current waveforms)

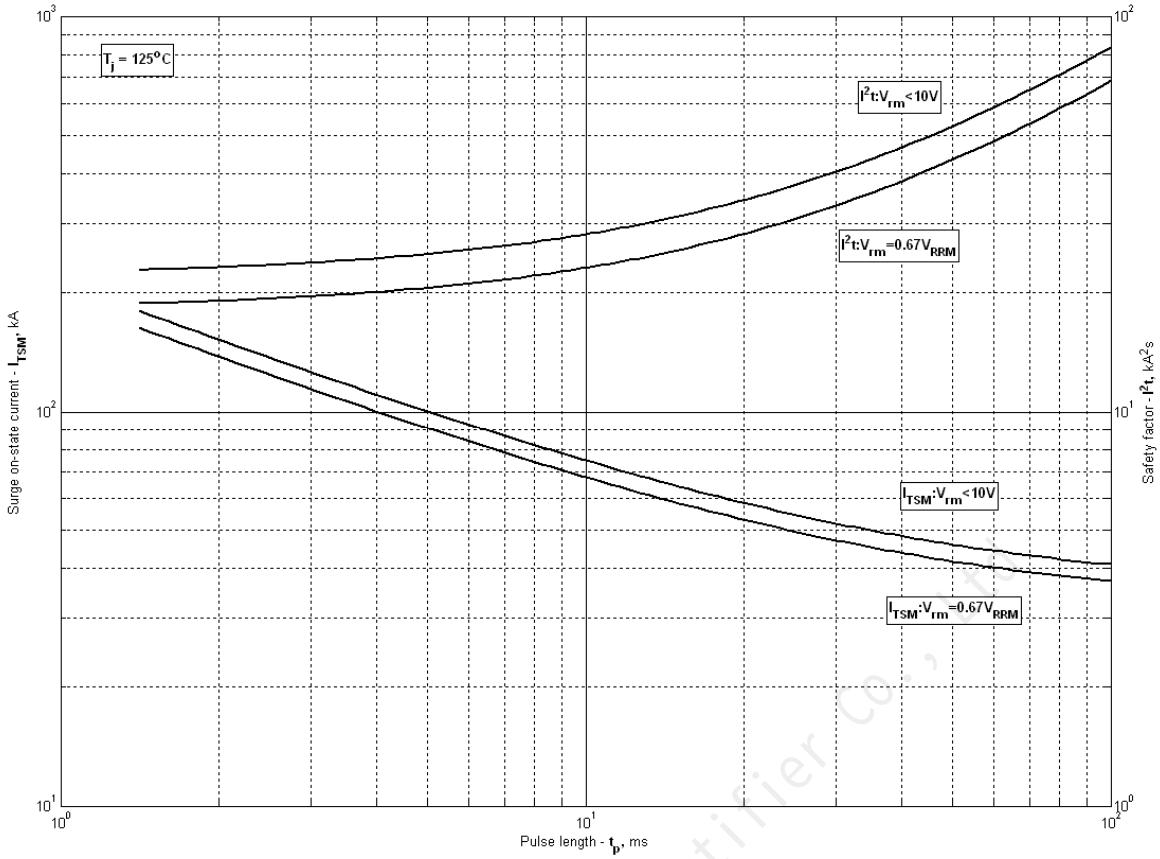


Fig 13 – Maximum surge and I^2t ratings

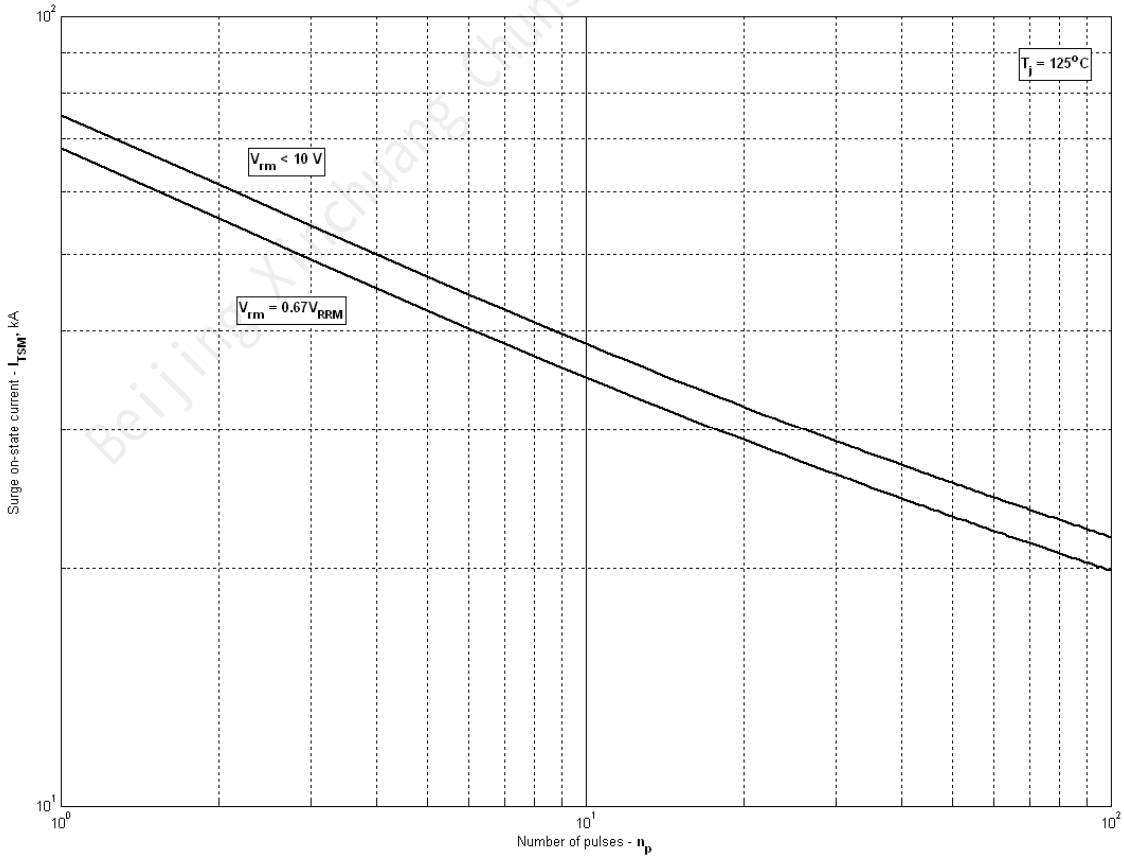


Fig 14 – Maximum surge ratings

