High-end Power Semiconductor Manufacturer

CSG25J4500

Gate Turn-off Thyristor

APPLICATIONS

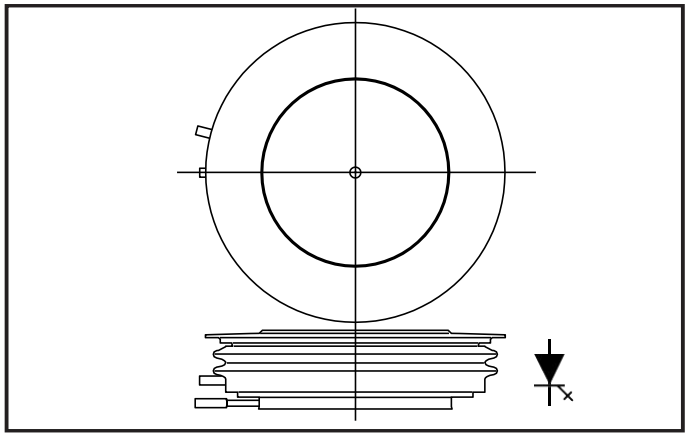
- Variable speed A.C. motor drive inverters (VSD-AC).
- Uninterruptable Power Supplies.
- High Voltage Converters.
- Choppers.
- DC/DC Converters.

KEY PARAMETERS

I_{TCM}	2500A
V_{DRM}	4500V
V_{TM}	3.4 V
di_T/dt	400A/μs

FEATURES

- Double Side Cooling.
- High Reliability In Service.
- High Voltage Capability.
- Fault Protection Without Fuses.
- High Surge Current Capability.
- Turn-off Capability Allows Reduction In Equipment Size And Weight.
- Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements.



Outline type code: J .
See Package Details for further information.

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
CSG25J4500	4500	16	Tj = 125℃,VGK= - 2V

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	V_{DM} = 4500V, Tj = 125℃, di_{GQ}/dt = 50A/μs, Cs = 6μF	2500	A
$I_{T(RMS)}$	RMS on-state current	T_{HS} = 77℃. Double side cooled. Half sine 50Hz.	1200	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. Tj = 125℃	16.0	kA
di/dt	Critical rate of rise of on-state current	V_D = 50% V_{DRM},Tj = 125℃, I_{GM}=25A	400	A/μs
dv/dt	Rate of rise of off-state voltage	To 66% $V_{DRM,}$ Tj = 125℃, VGK=-2V	1000	V/μs

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		-	100	A
$P_{FG(AV)}$	Average forward gate power		-	50	W
$P_{RG(AV)}$	Peak reverse gate power		-	150	W
di_{GQ}/dt	Rate of rise of reverse gate current		30	60	A/μs

THERMAL RATINGS AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.0146	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 35.0kN With mounting compound	per contact	-	0.0036	°C/W
T_{vj}	Virtual junction temperature			-40	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	°C
-	Clamping force			30.0	38.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Units**
V_{TM}	On-state voltage	At 2500A peak, Tj = 125℃	-	3.4	V
I_{DM}	Peak off-state current	V_{DRM} = 4500V, V_{RG} = 0V	-	100	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.5	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	3.5	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	10	mA
E_{ON}	Turn-on energy	V_D = 2250V I_T = 2500A, dI_T/dt = 300A/μs I_{FG} = 40A, rise time < 1.0μs	-	3000	mJ
t_d	Delay time		-	3	μs
t_r	Rise time		-	3.0	μs
E_{OFF}	Turn-off energy	I_T = 2500A, V_{DM} = 4500V Snubber Cap Cs = 6.0μF, di_{GQ}/dt = 50A/μs	-	6300	mJ
t_{gs}	Storage time		-	23	μs
t_{gf}	Fall time		-	10	μs
t_{gq}	Gate controlled turn-off time		-	25	μs
I_{GQM}	Peak reverse gate current		650	-	A

CURVES

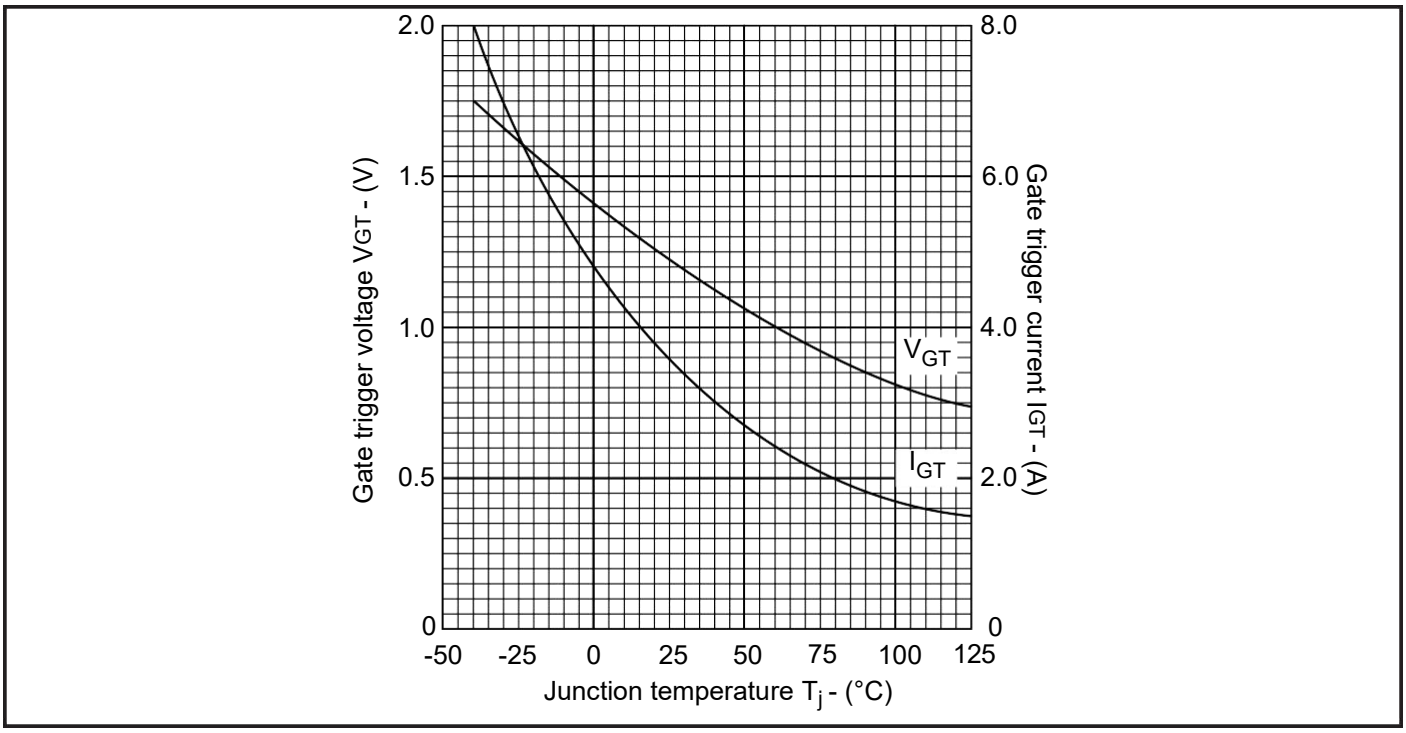


Fig.1 Maximum gate trigger voltage/current vs junction temperature

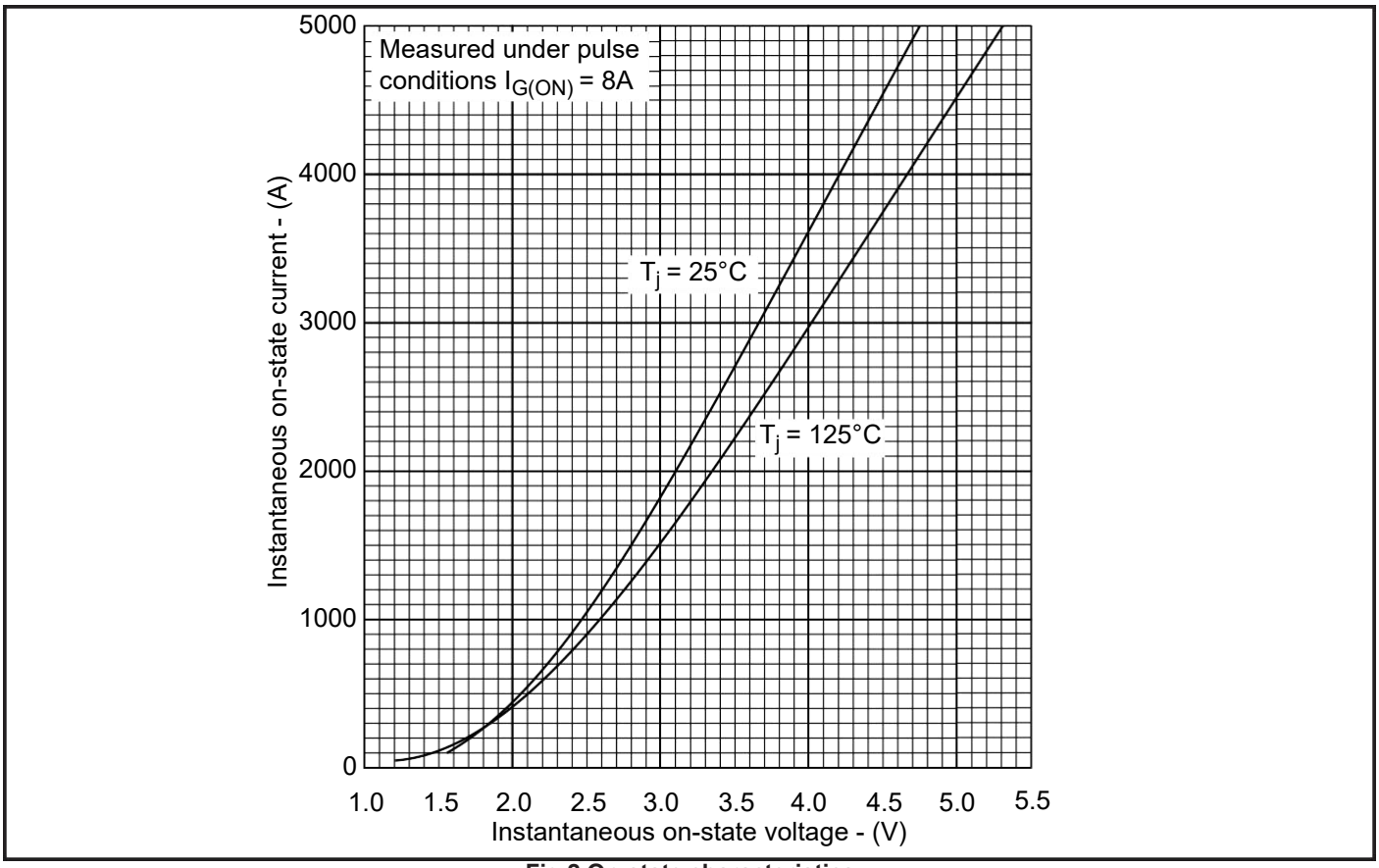


Fig.2 On-state characteristics

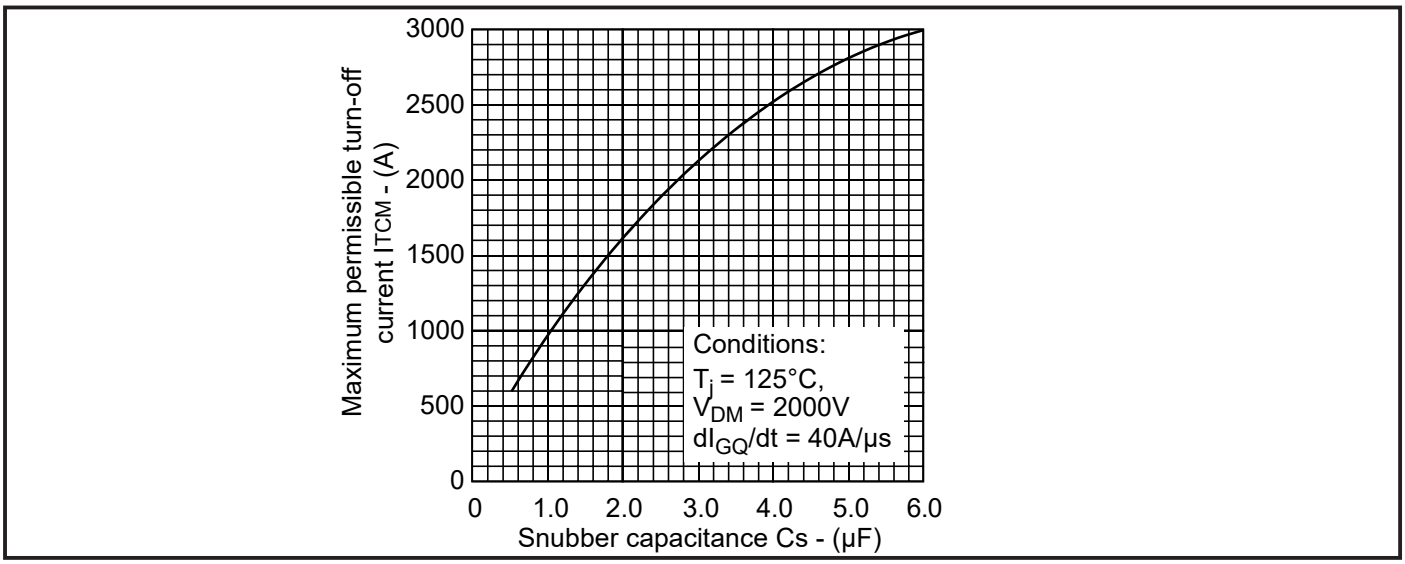


Fig.3 Maximum dependence of I_{TCM} on C_S

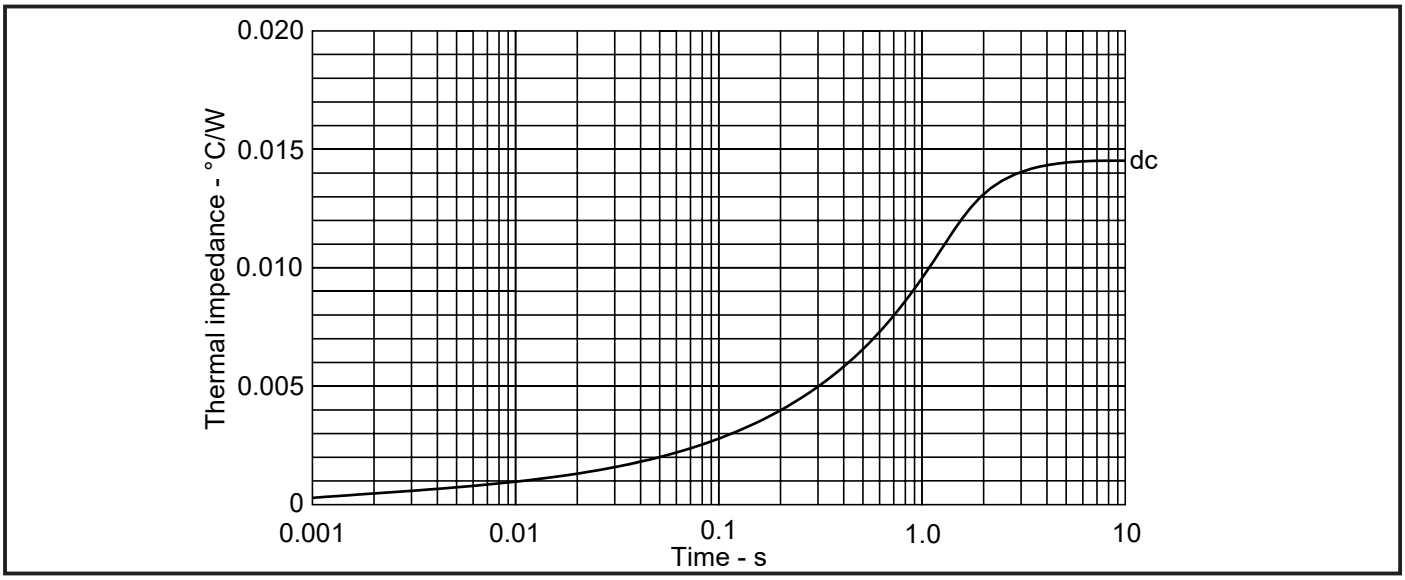


Fig.4 Maximum (limit) transient thermal impedance - double side cooled

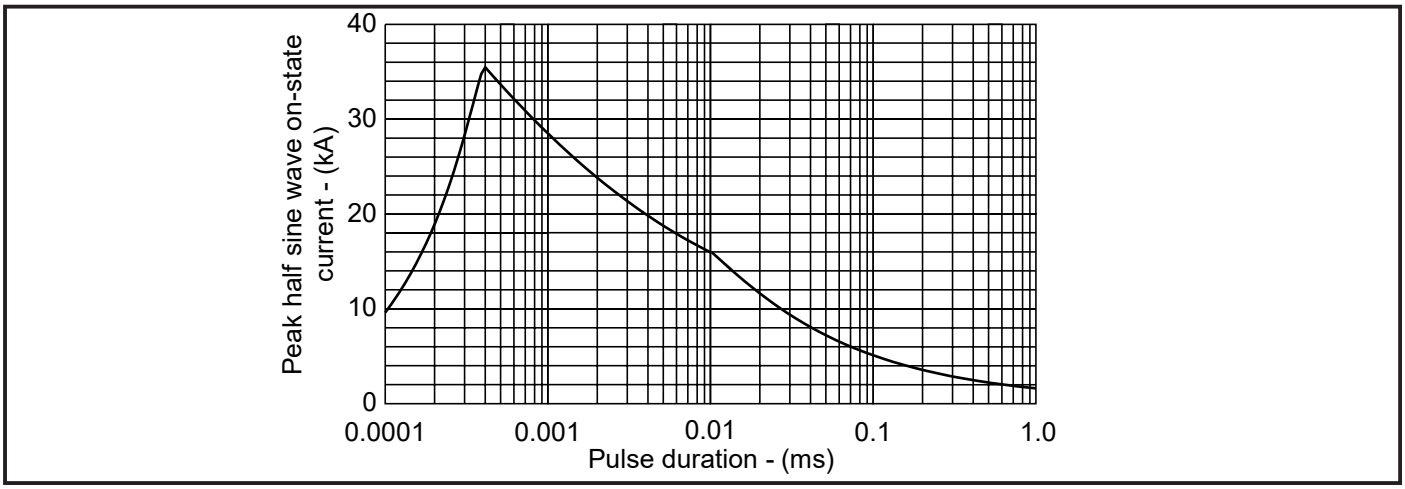


Fig.5 Surge (non-repetitive) on-state current vs time

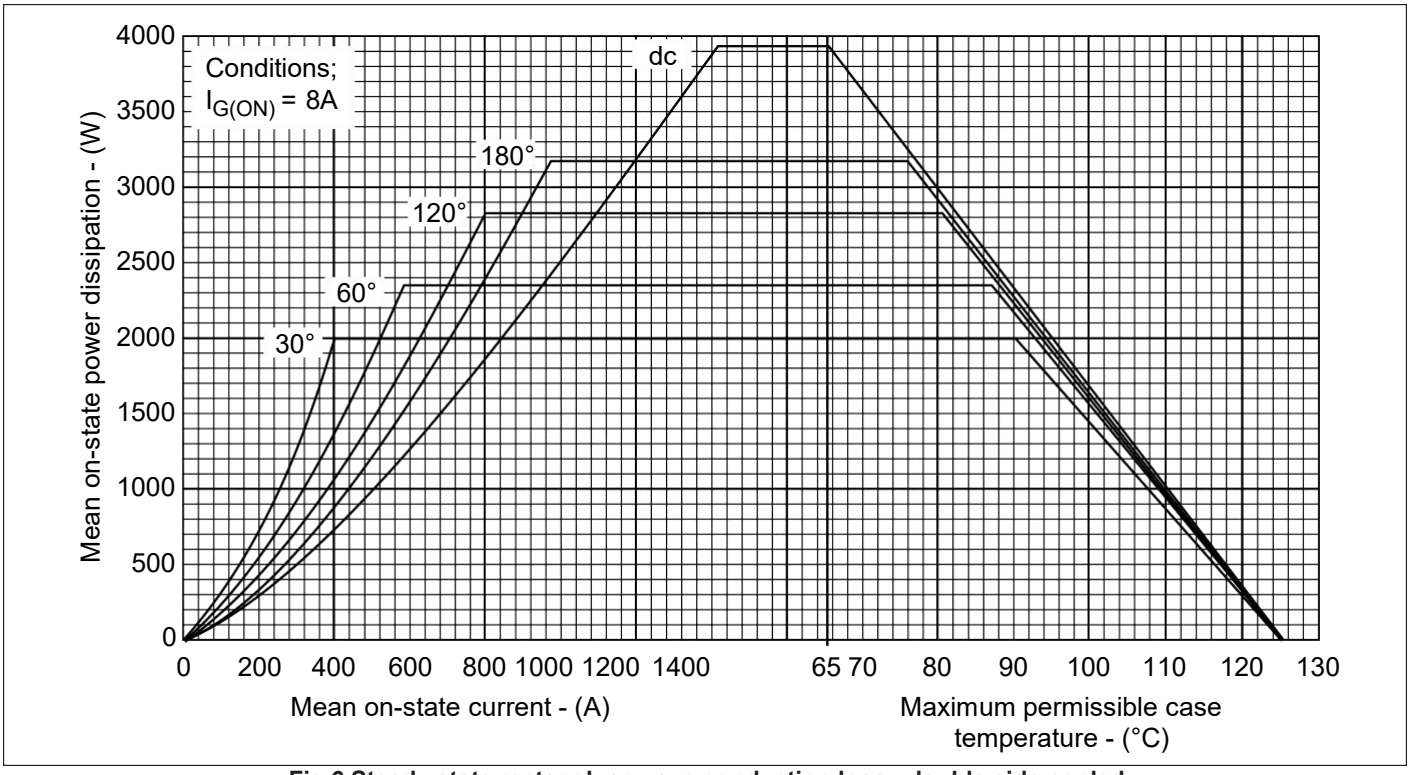


Fig.6 Steady state rectangluar wave conduction loss - double side cooled

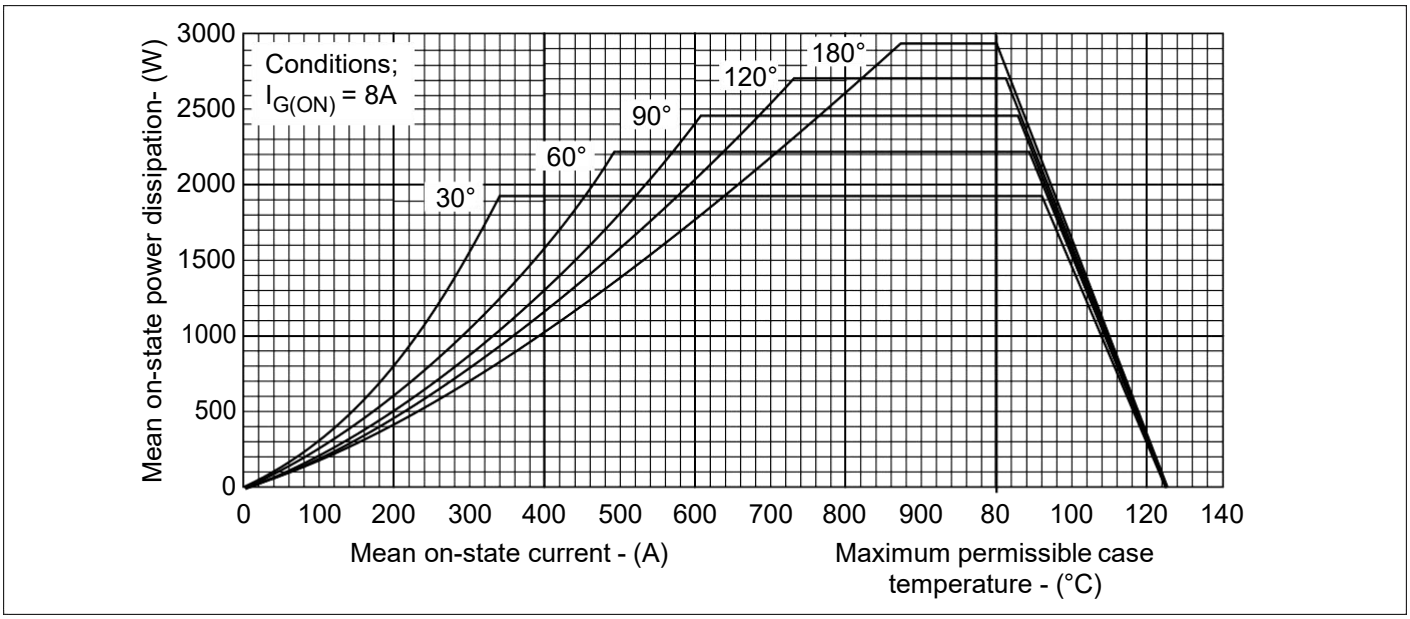


Fig.7 Steady state sinusoidal wave conduction loss - double side cooled

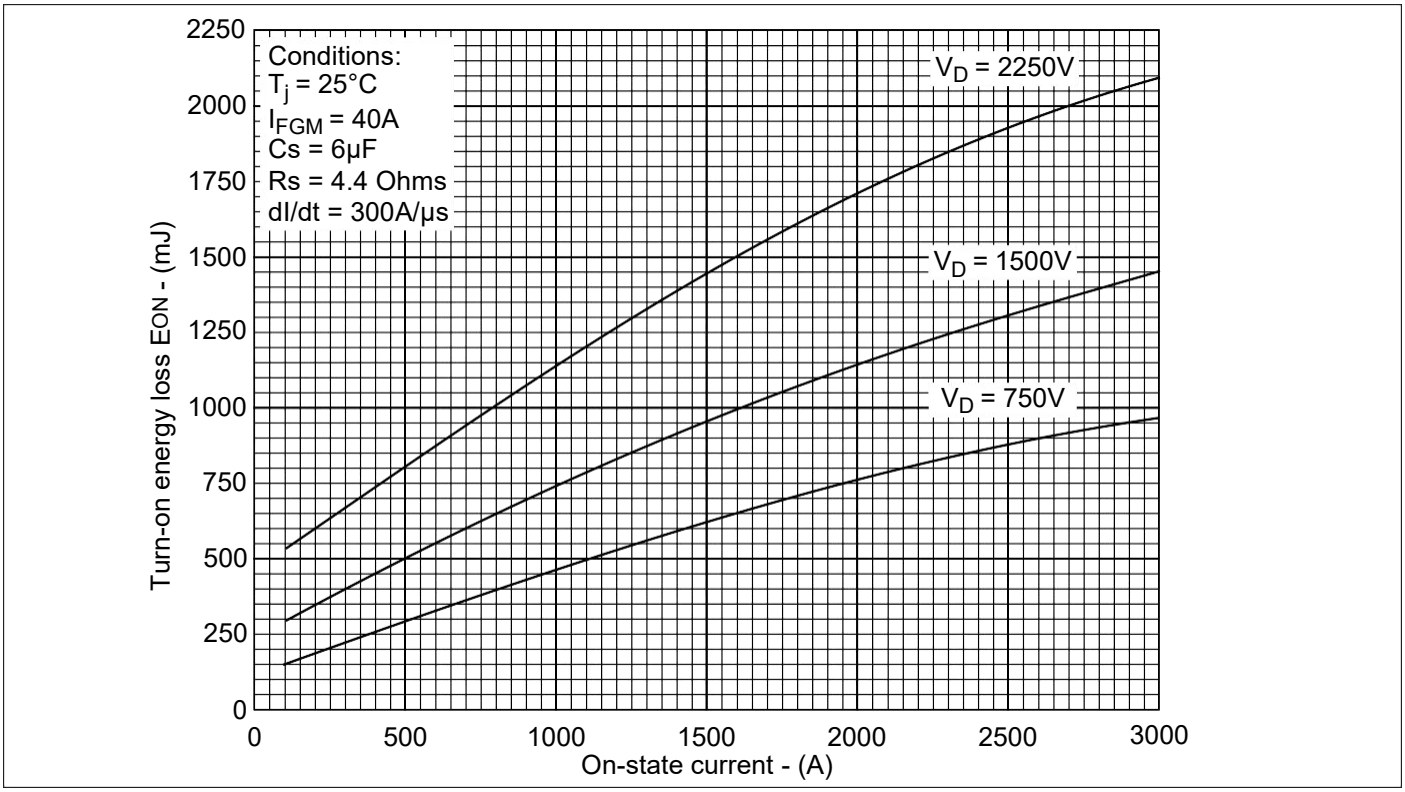


Fig.8 Turn-on energy vs on-state current

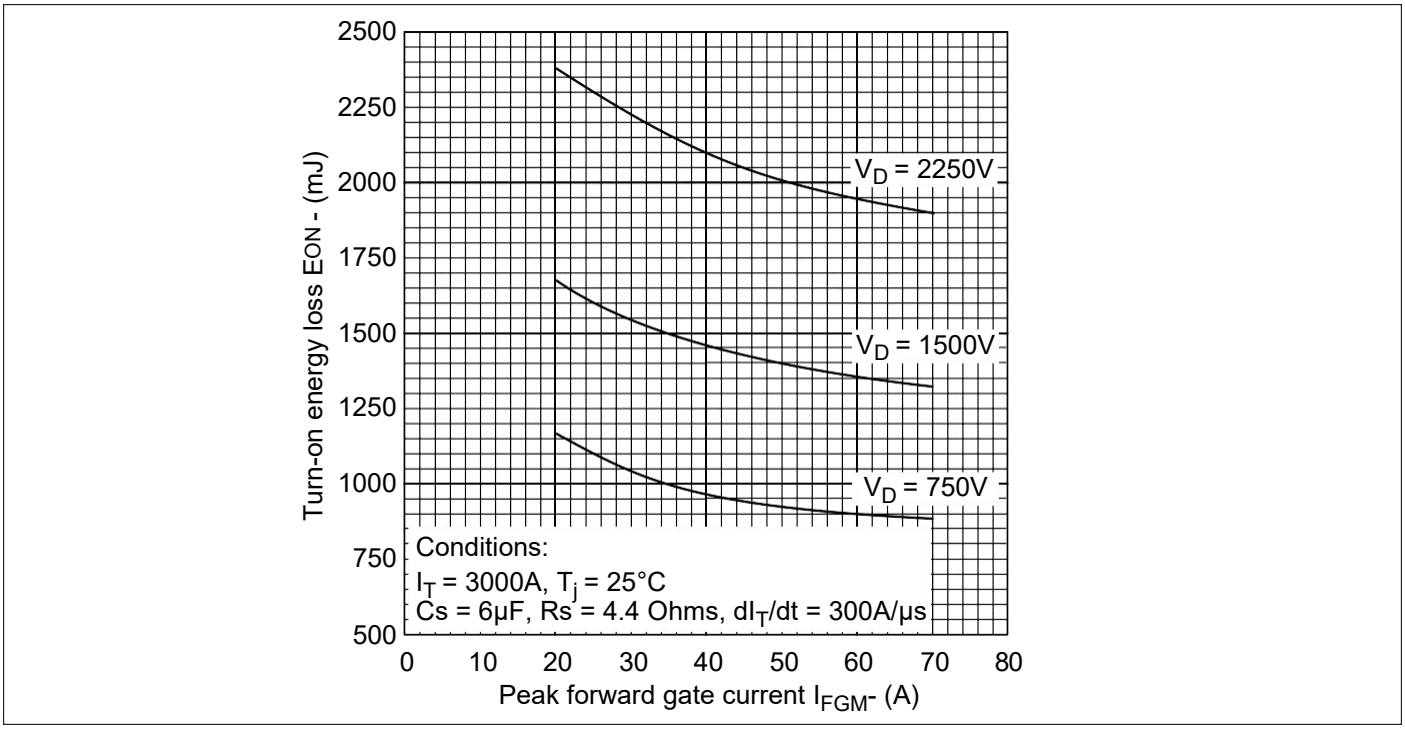


Fig.9 Turn-on energy vs peak forward gate current

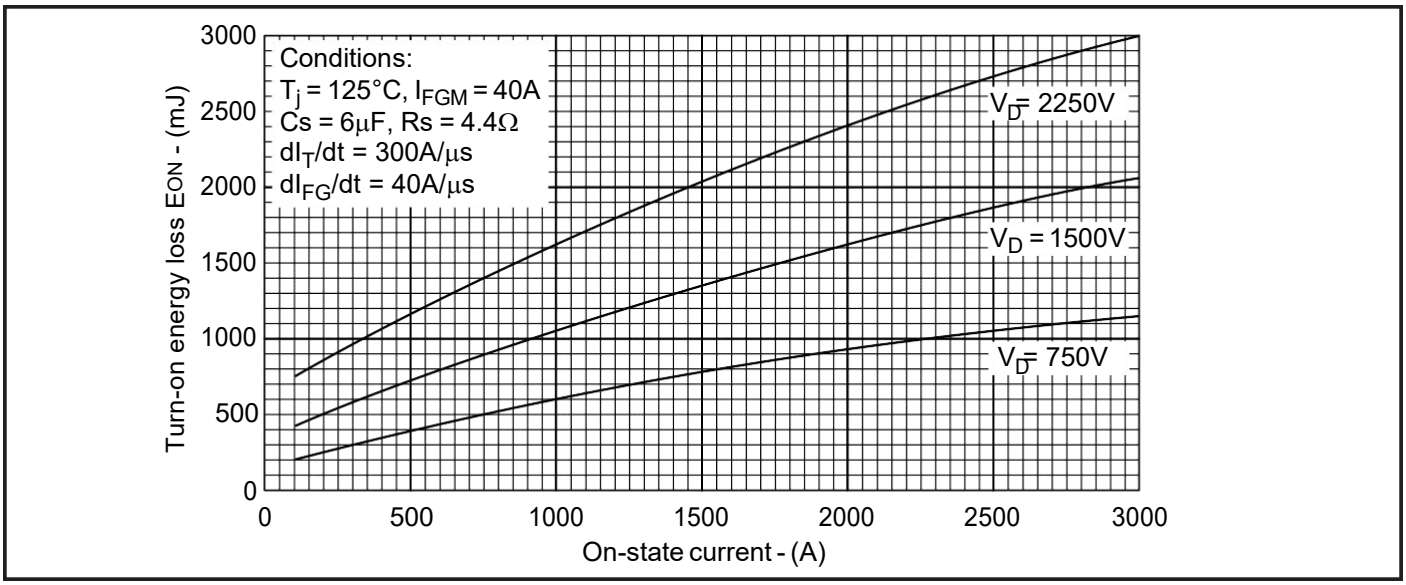


Fig.10 Turn-on energy vs on-state current

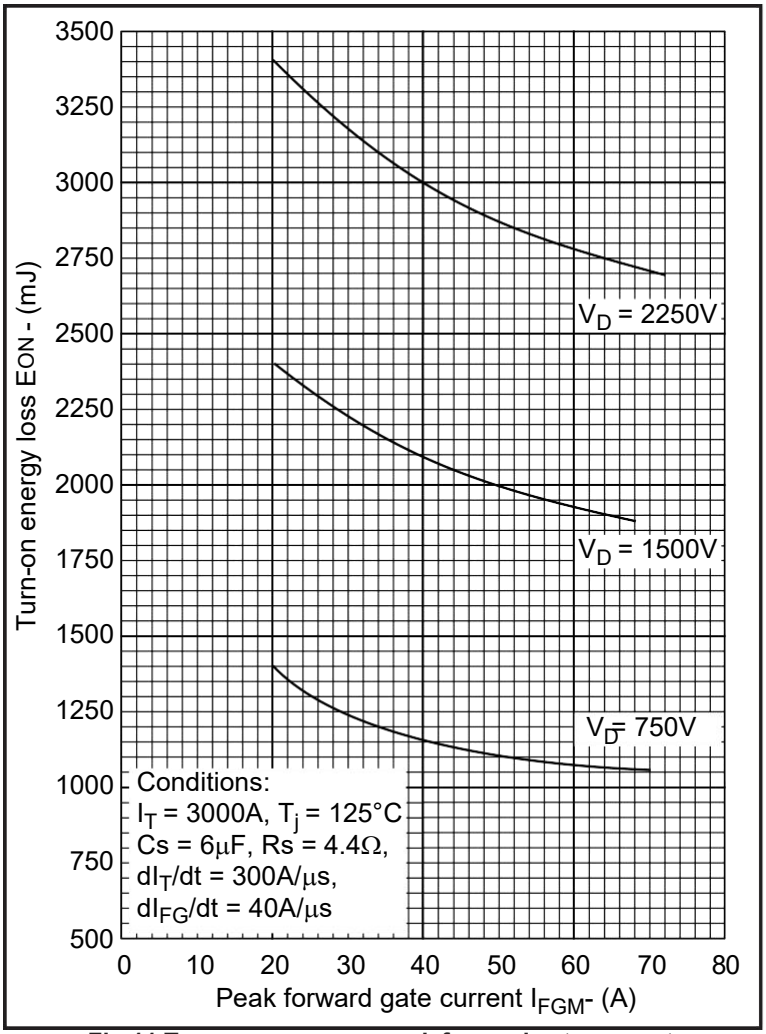


Fig.11 Turn-on energy vs peak forward gate current

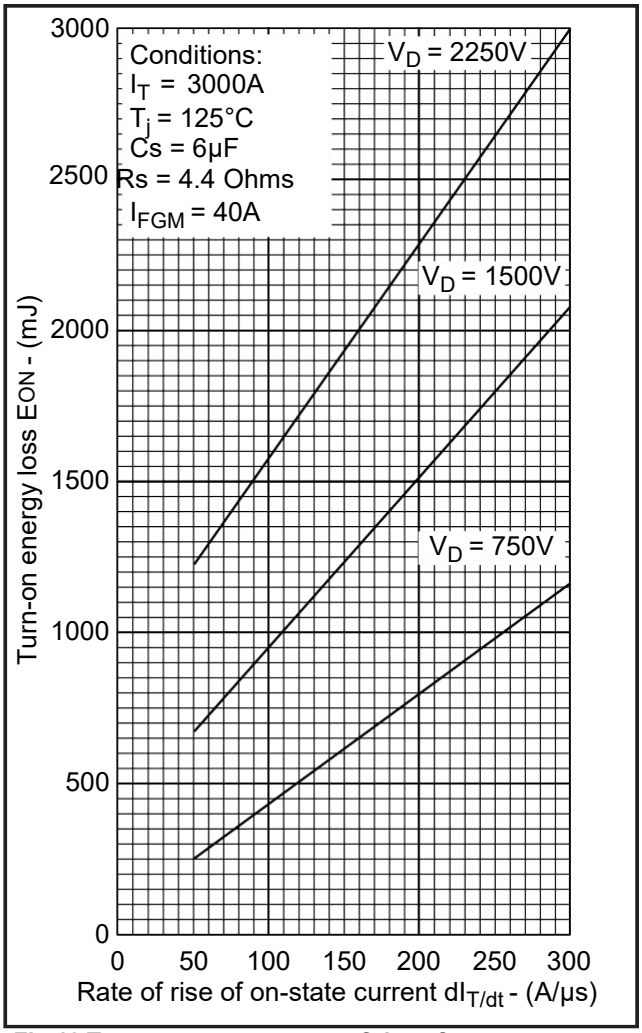


Fig.12 Turn-on energy vs rate of rise of on-state current

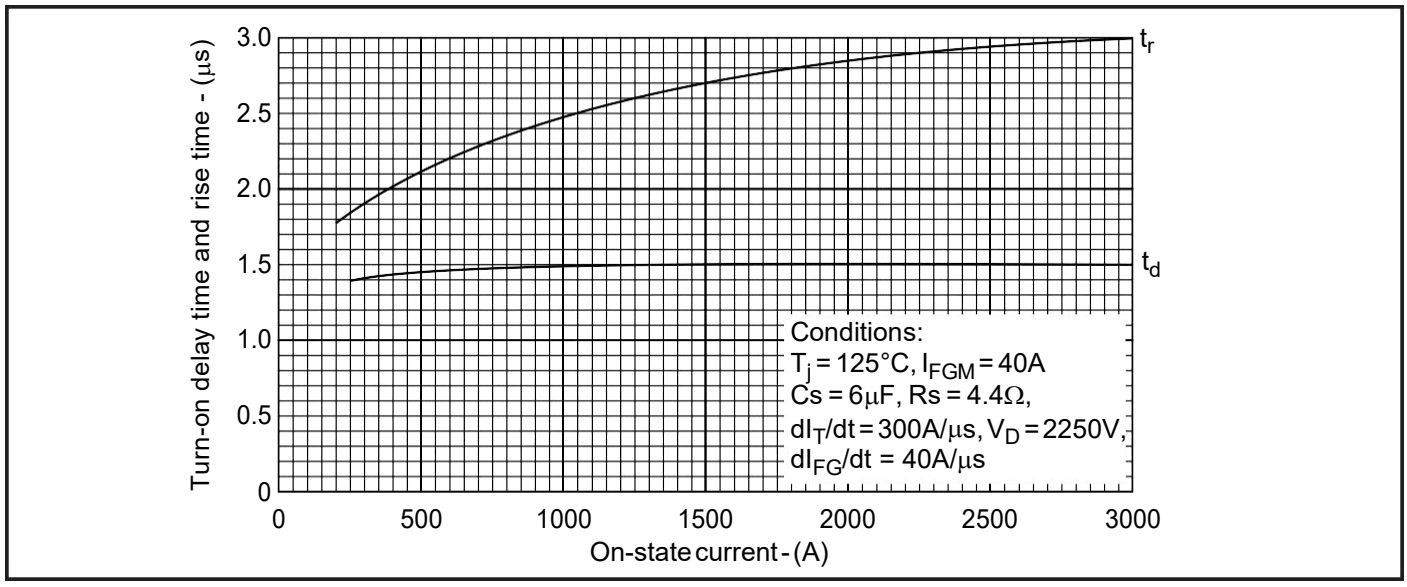


Fig.13 Delay time & rise time vs turn-on current

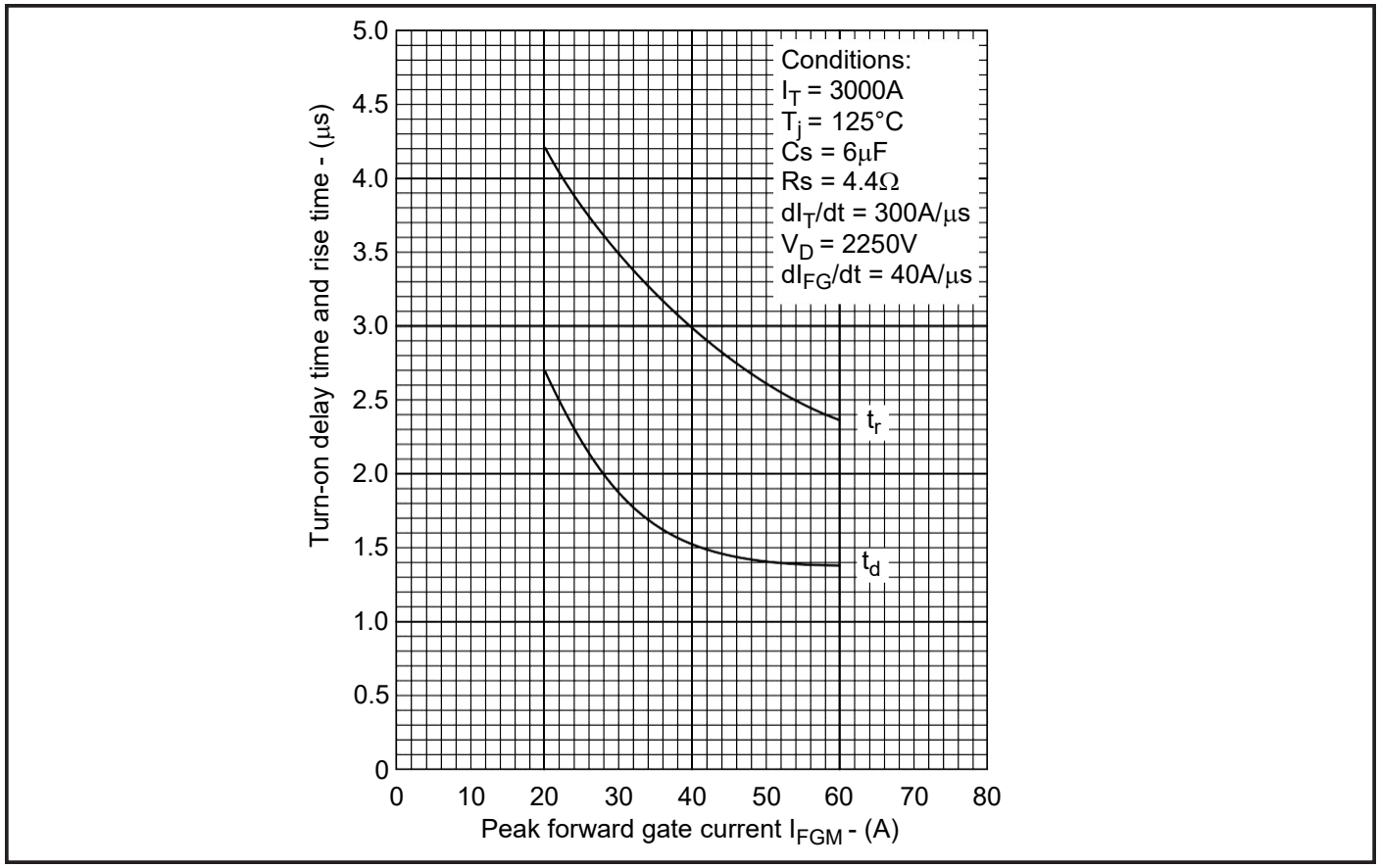


Fig.14 Delay time & rise time vs peak forward gate current

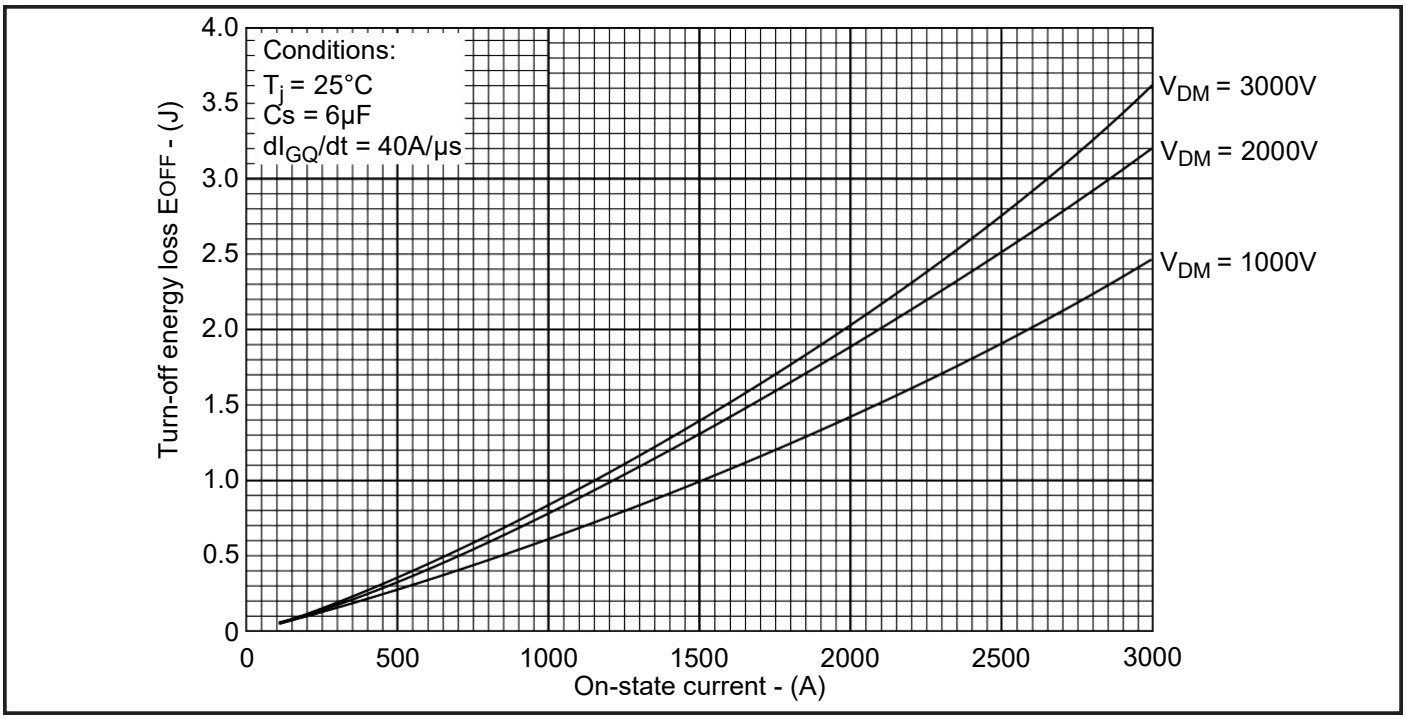


Fig.15 Turn-off energy vs on-state current

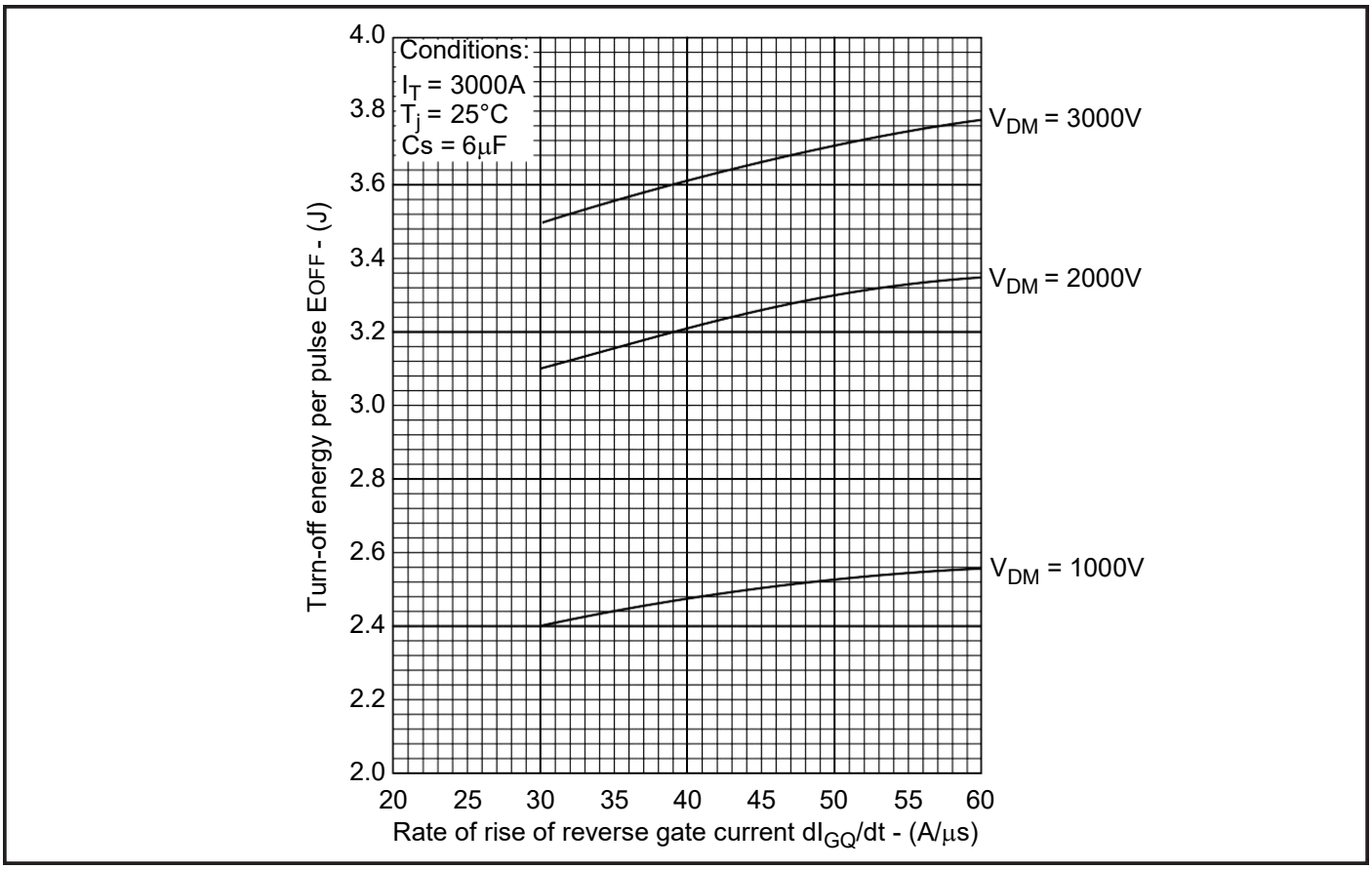


Fig.16 Turn-off energy vs rate of rise of reverse gate current

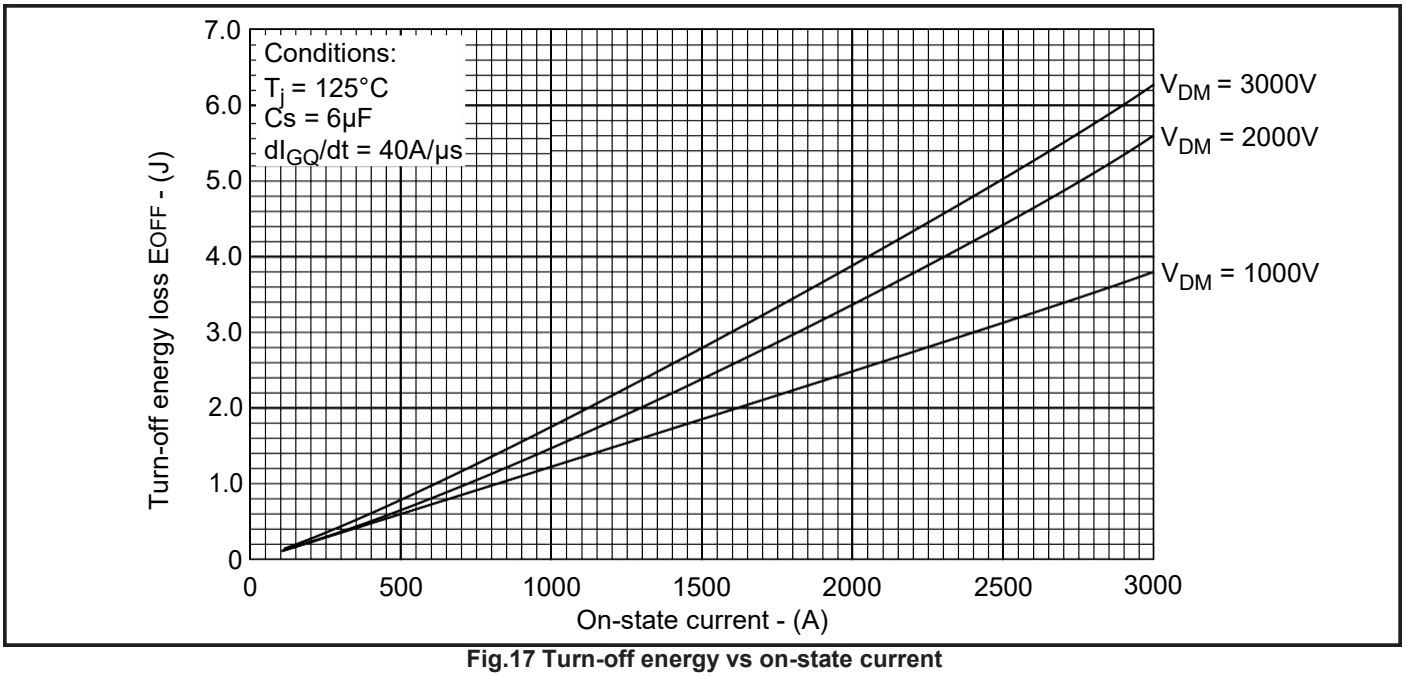


Fig.17 Turn-off energy vs on-state current

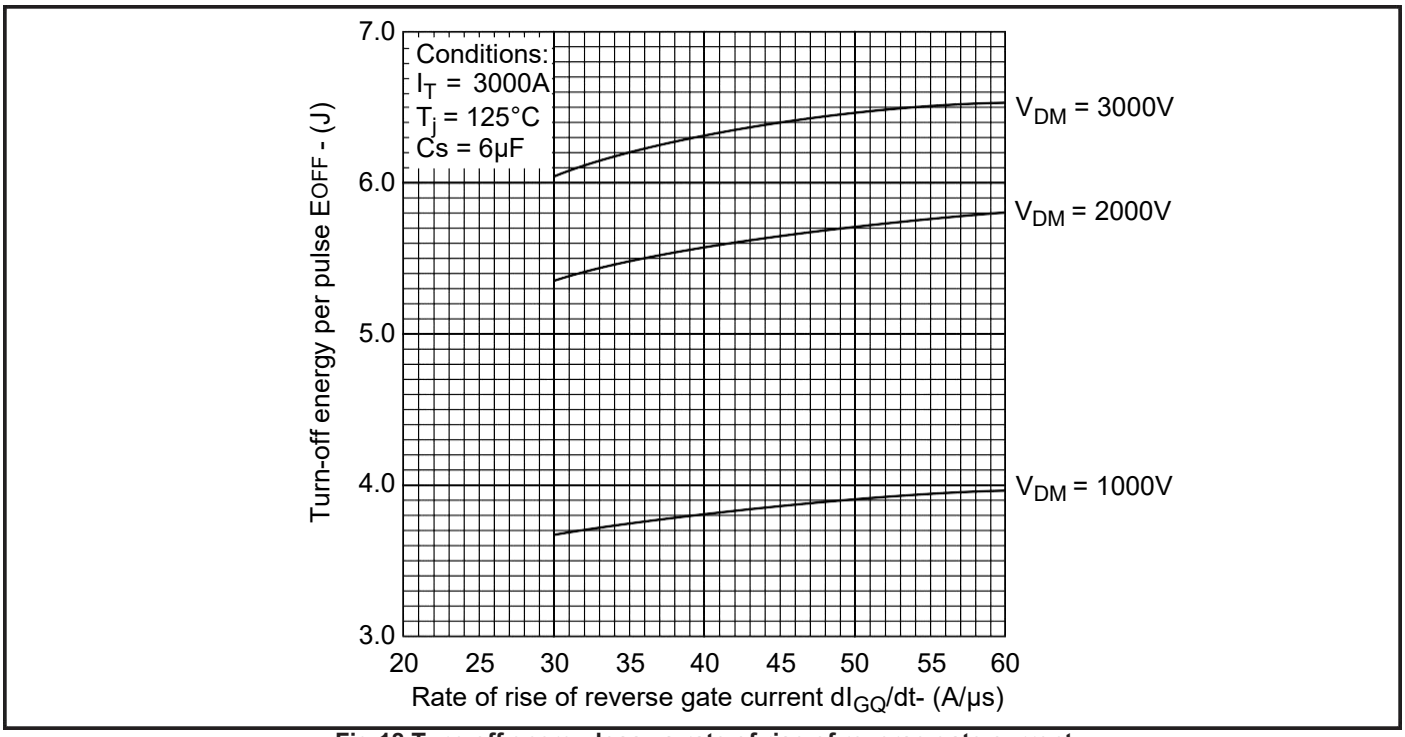


Fig.18 Turn-off energy loss vs rate of rise of reverse gate current

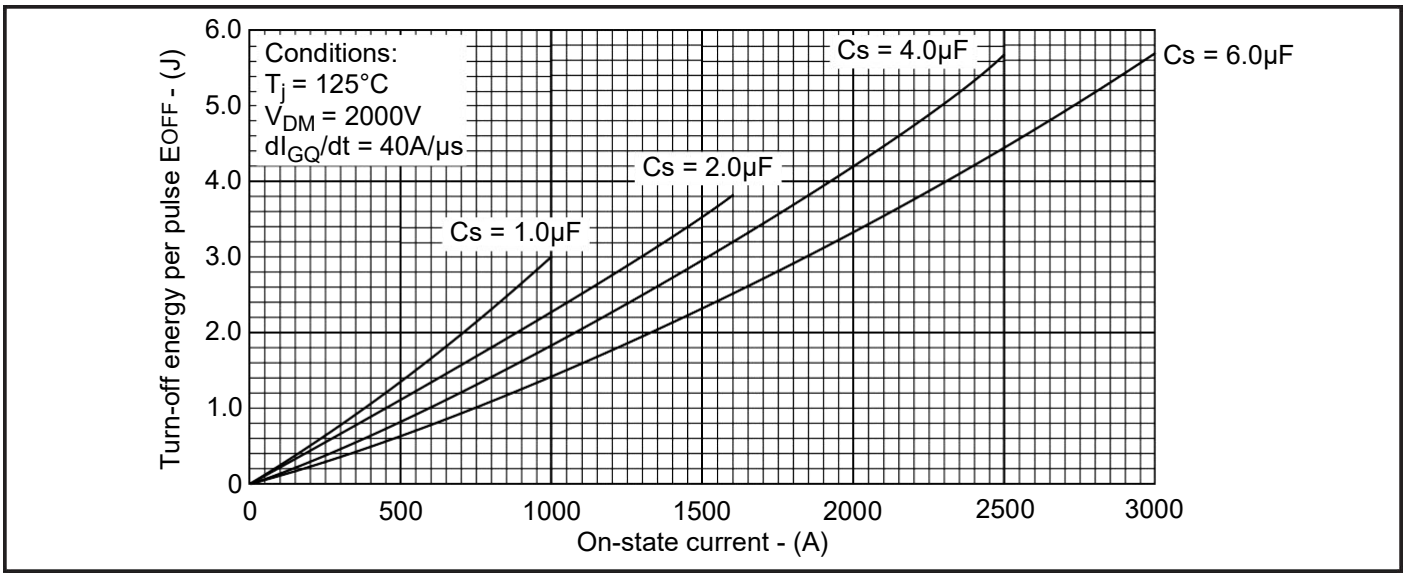


Fig.19 Turn-off energy vs on-state current

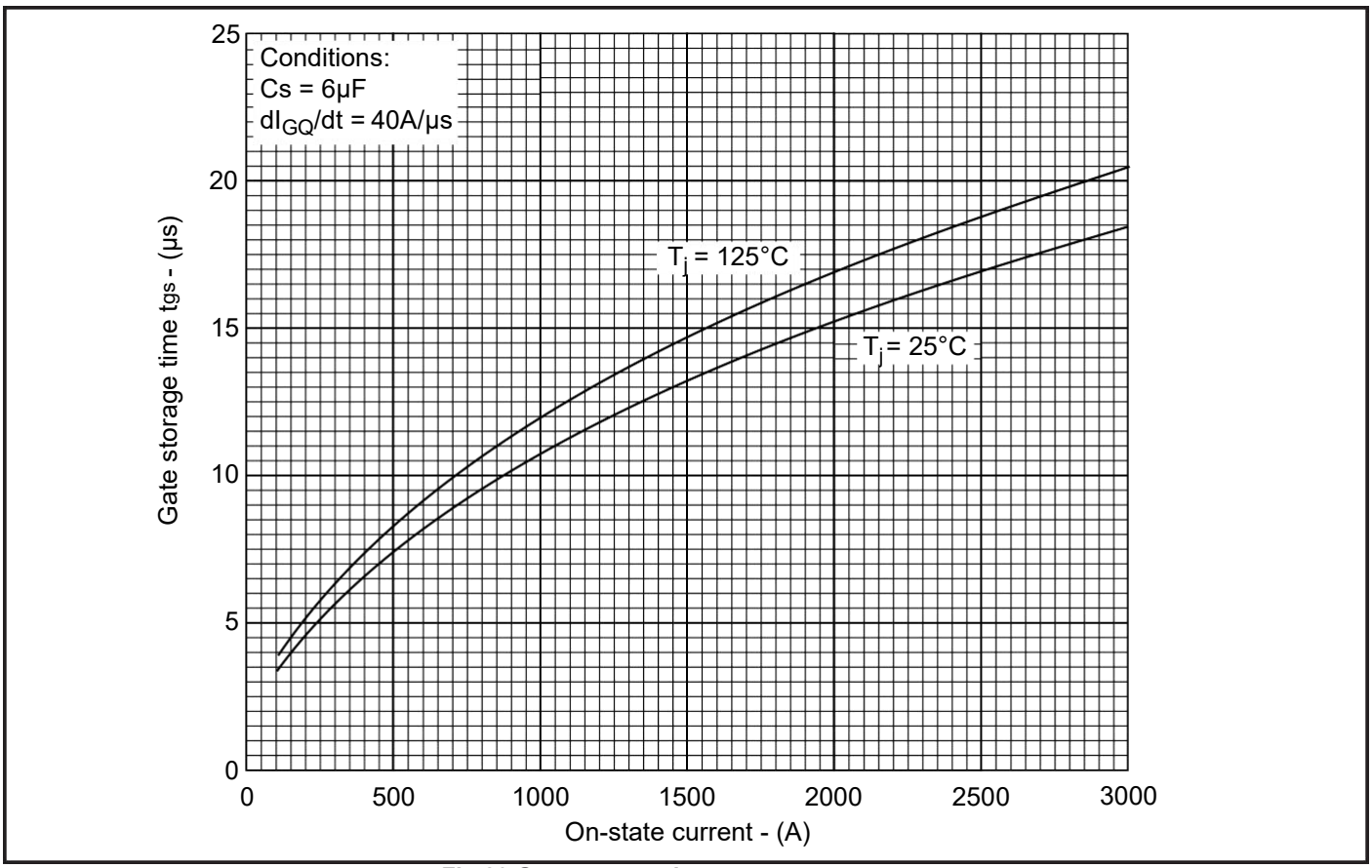


Fig.20 Gate storage time vs on-state current

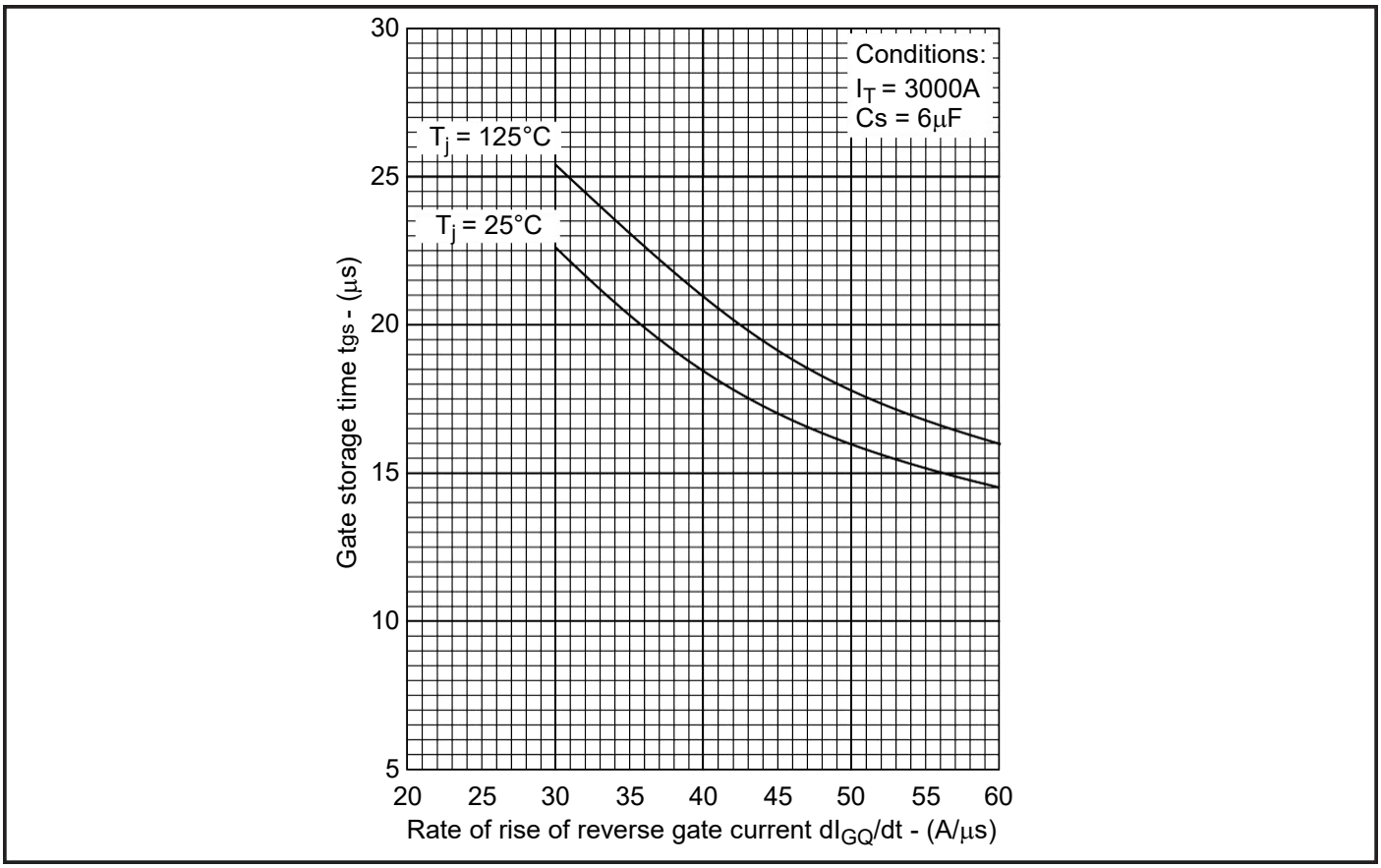


Fig.21 Gate storage time vs rate of rise of reverse gate current

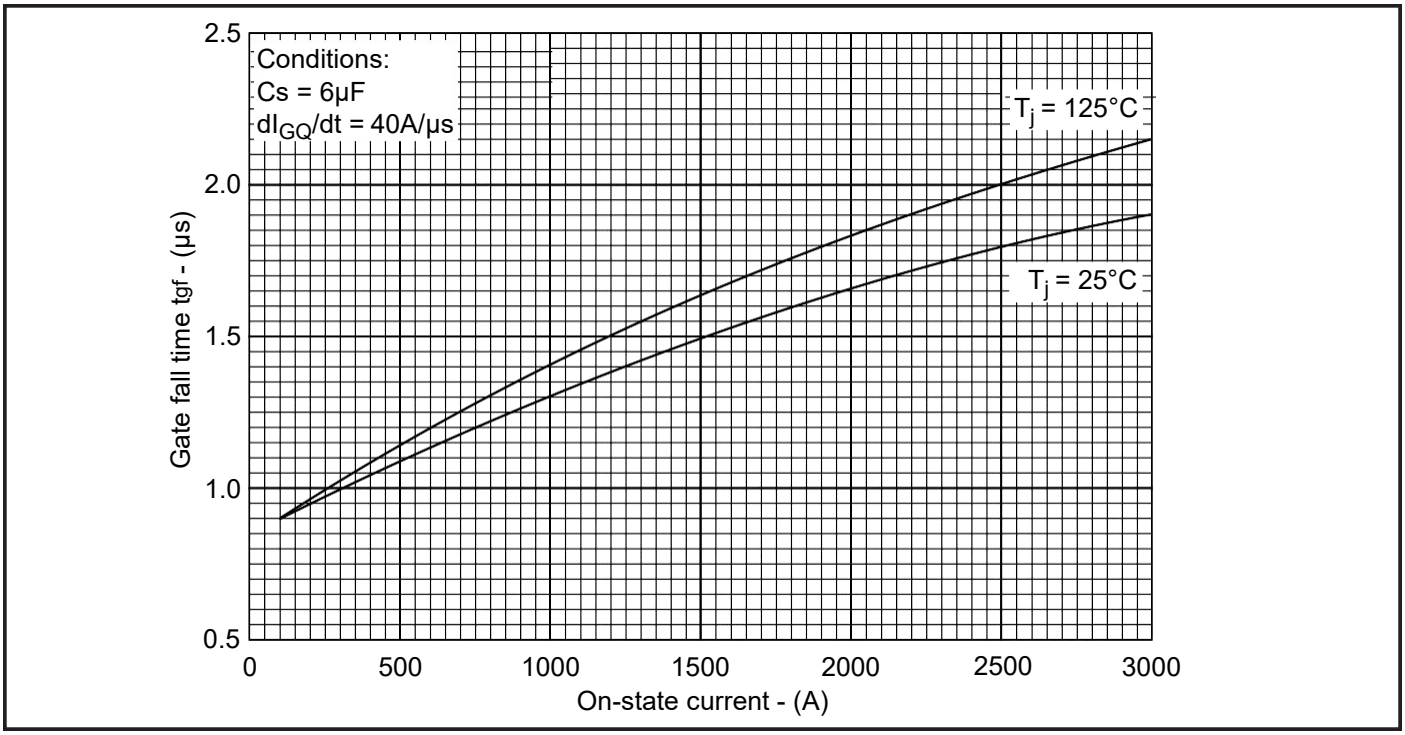


Fig.22 Gate fall time vs on-state current

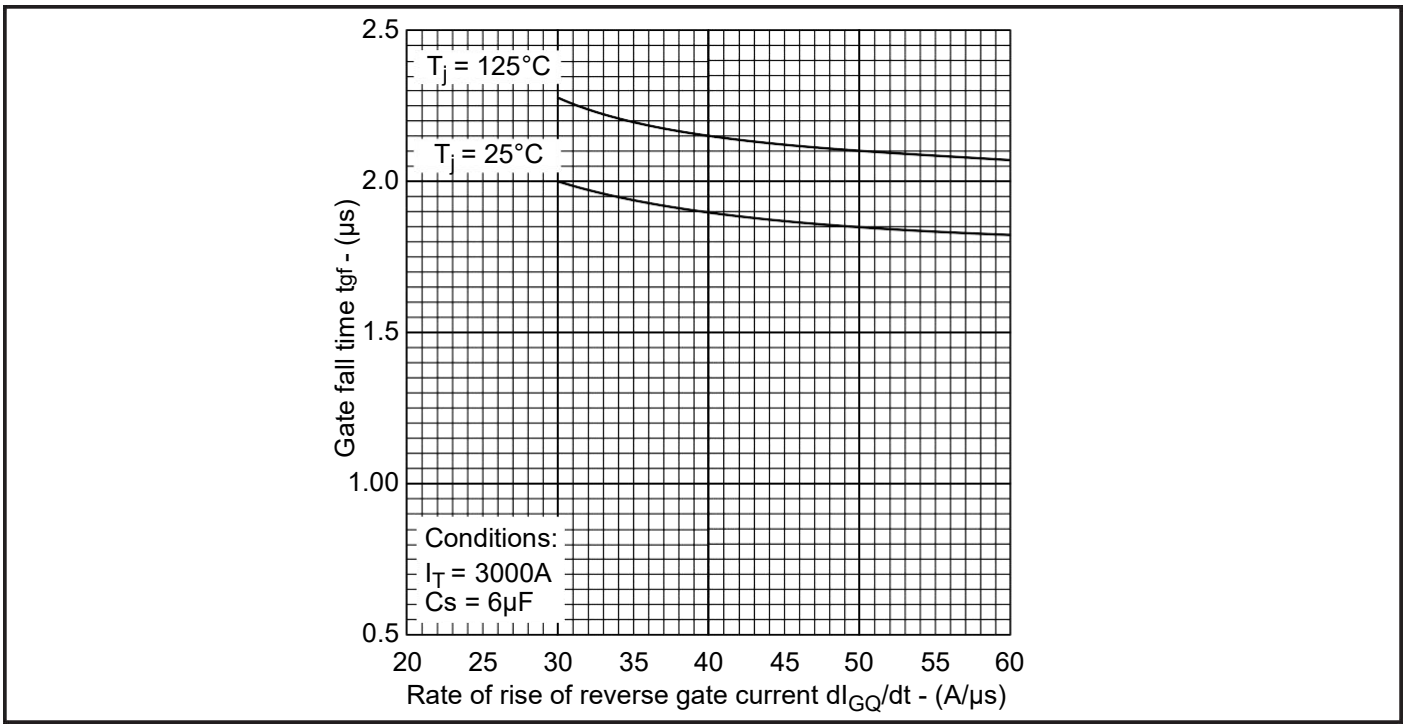


Fig.23 Gate fall time vs rate of rise of reverse gate current

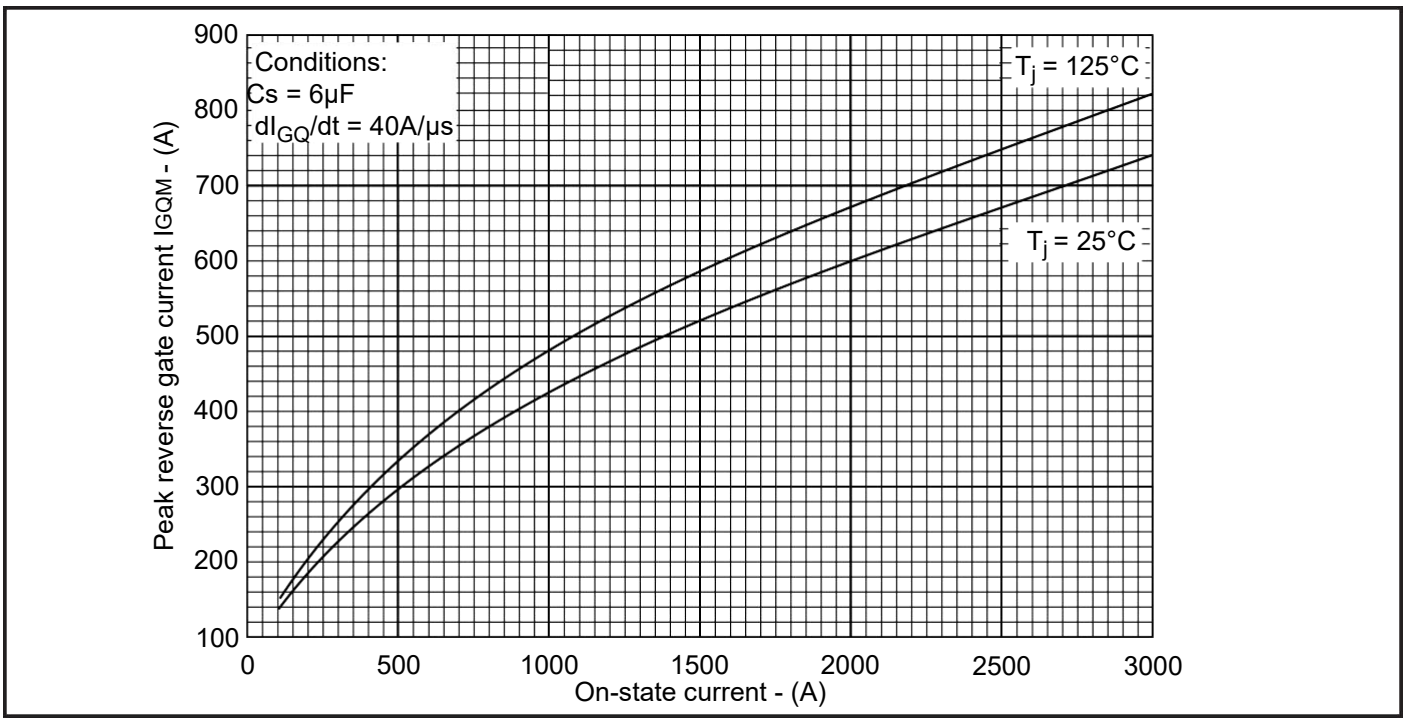


Fig.24 Peak reverse gate current vs turn-off current

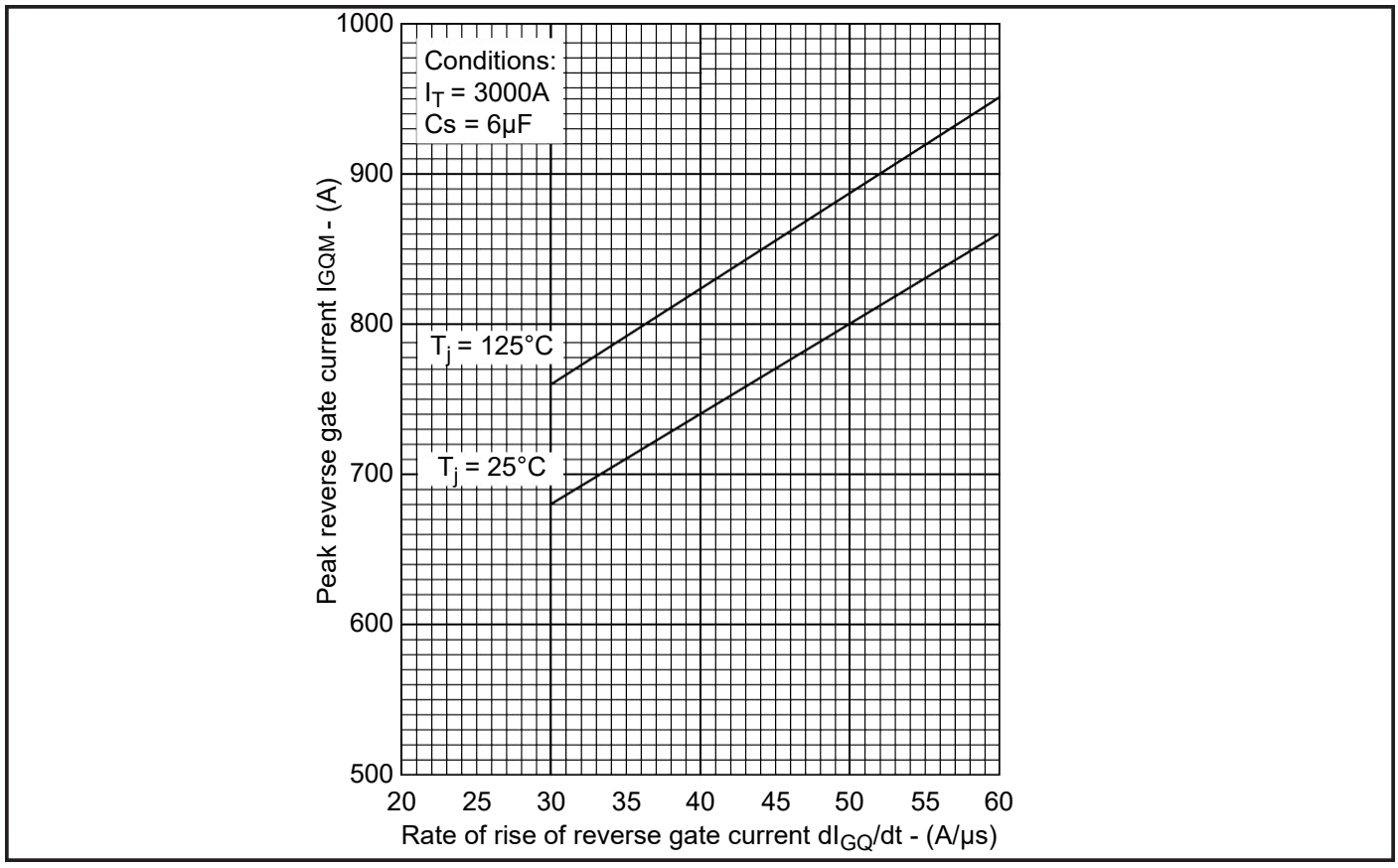


Fig.25 Peak reverse gate current vs rate of rise of reversegate current

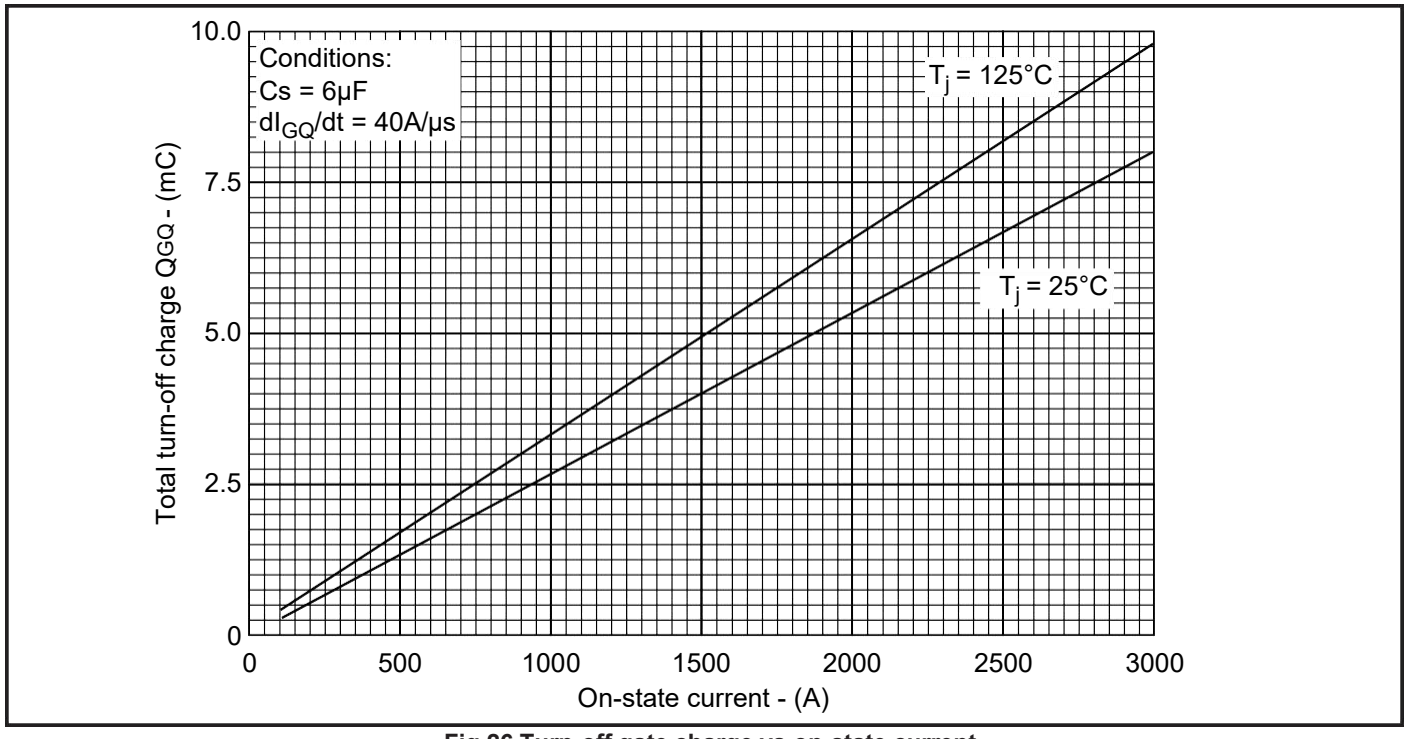


Fig.26 Turn-off gate charge vs on-state current

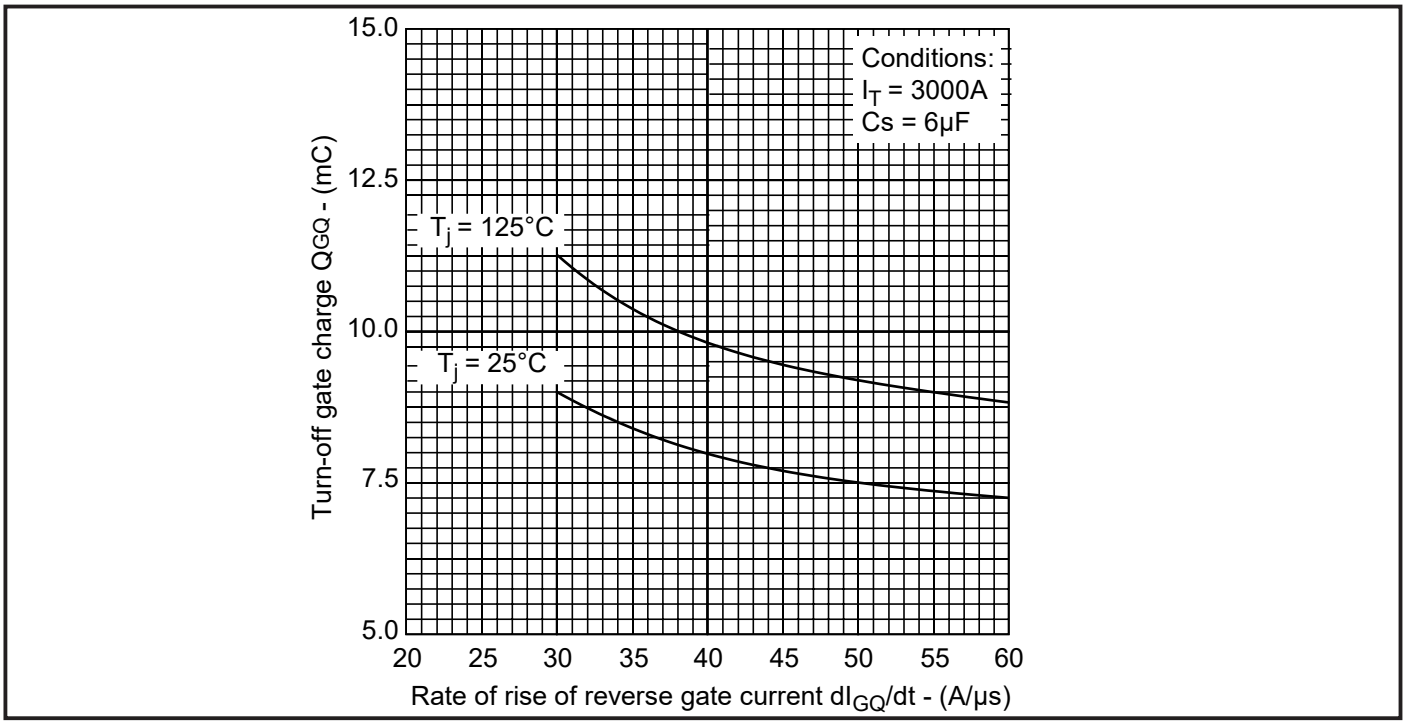


Fig.27 Turn-off gate charge vs rate of rise of reverse gate current

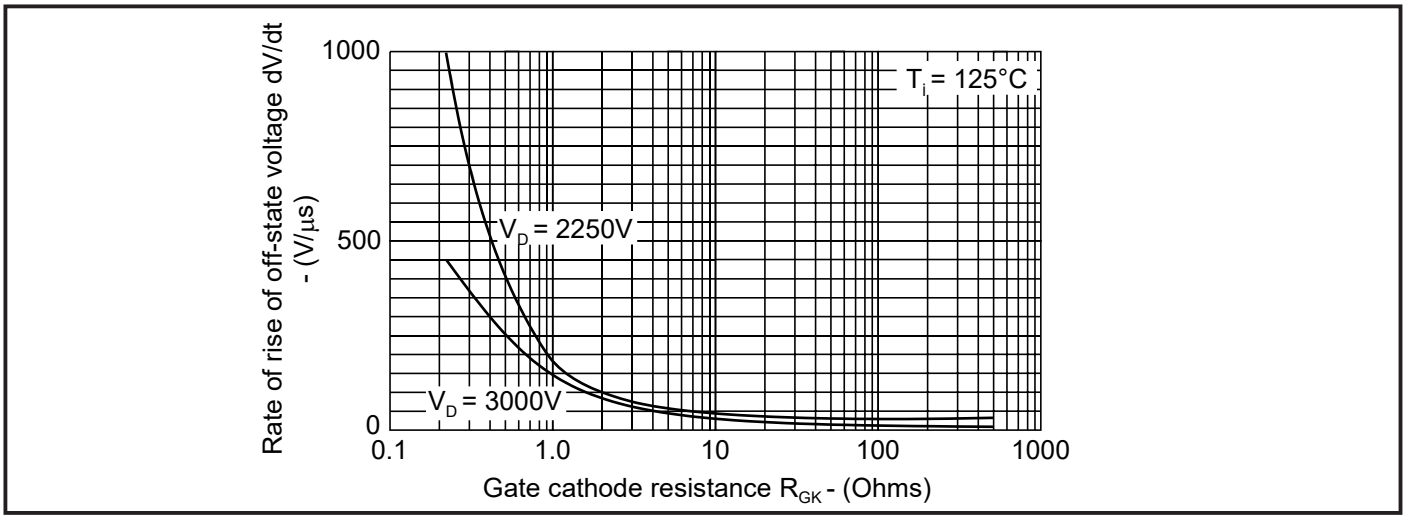
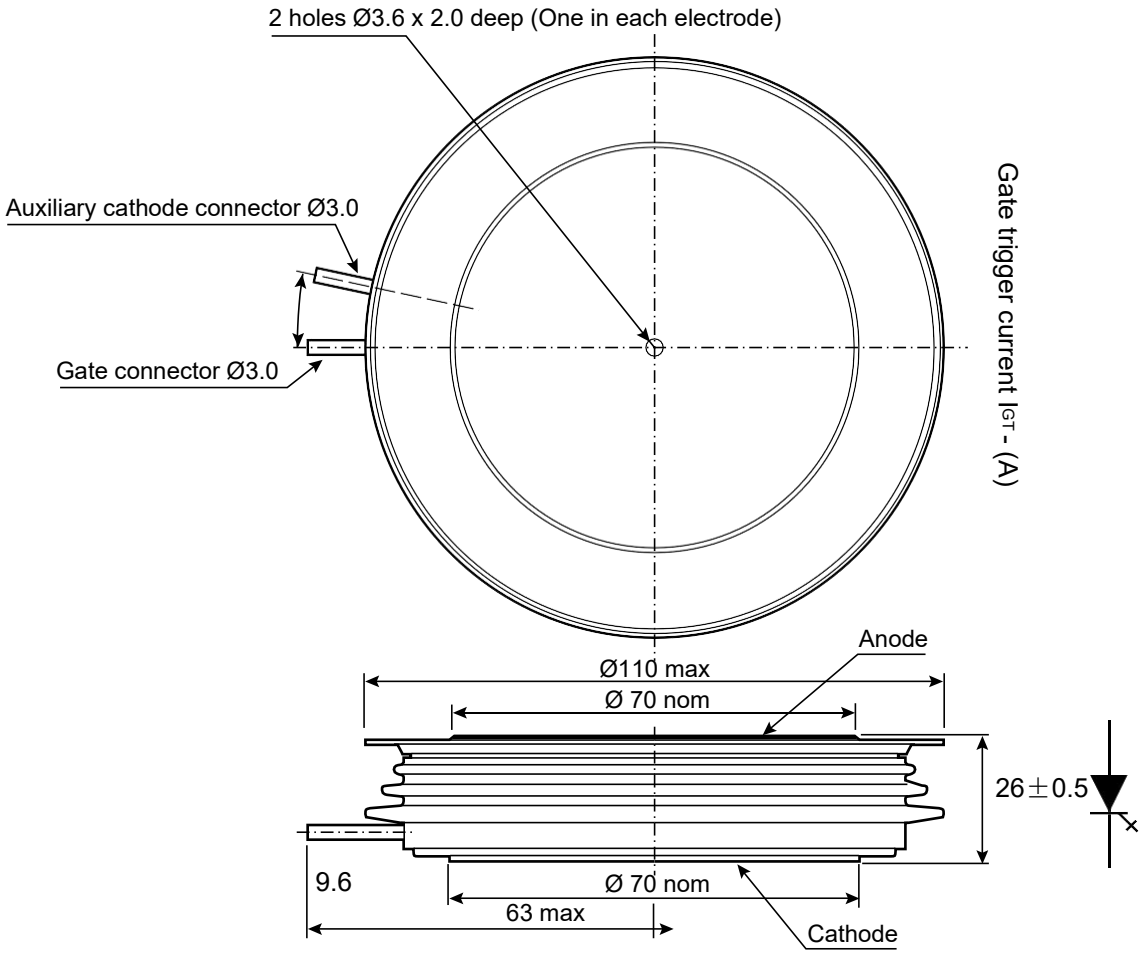


Fig.28 Rate of rise of off-state voltage vs gate cathode resistance

PACKAGE DETAILS

All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Package outline type code: J